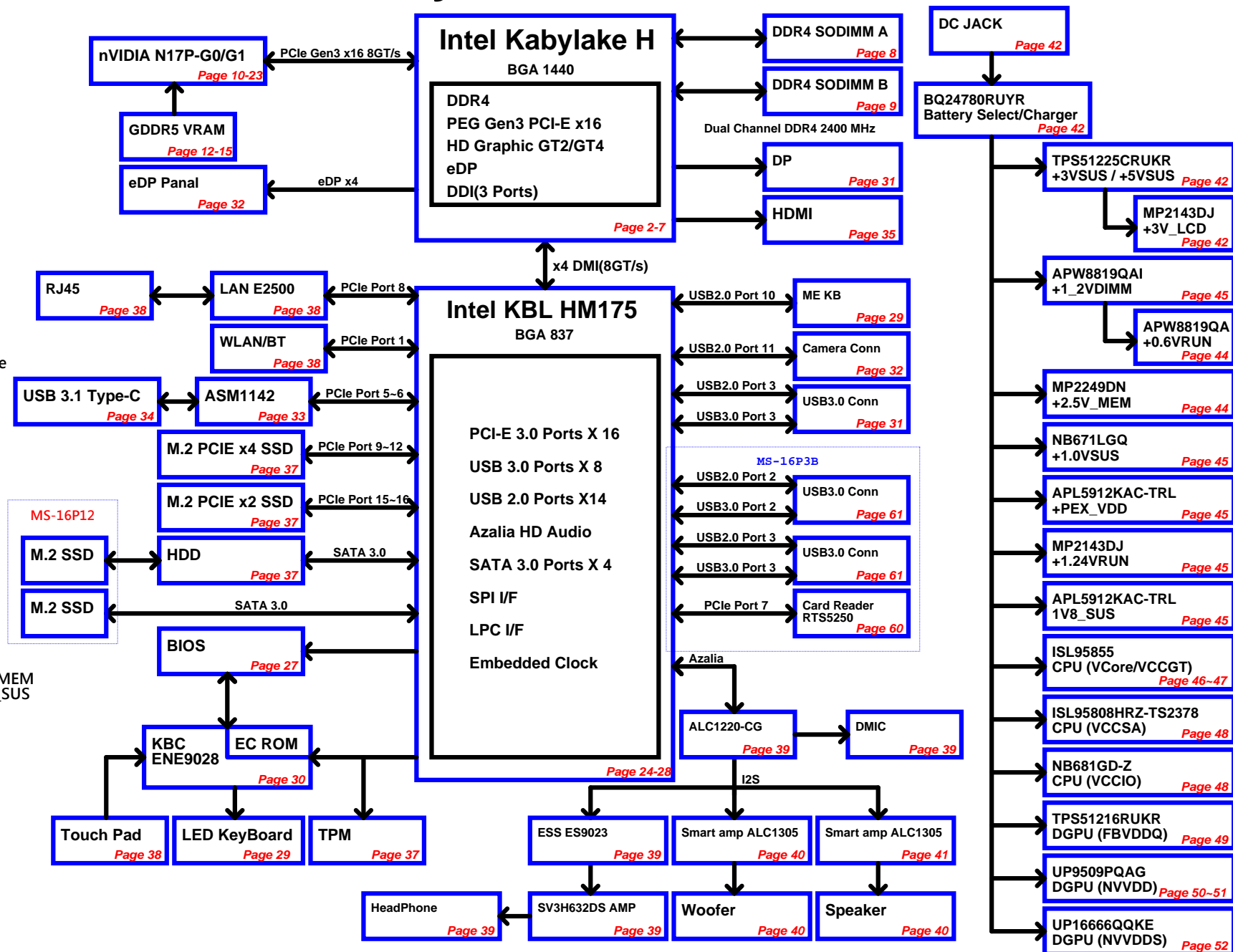


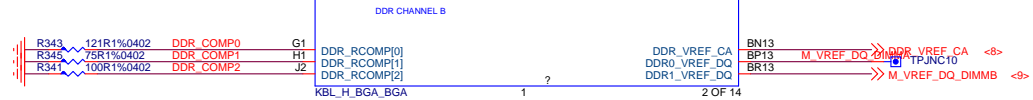
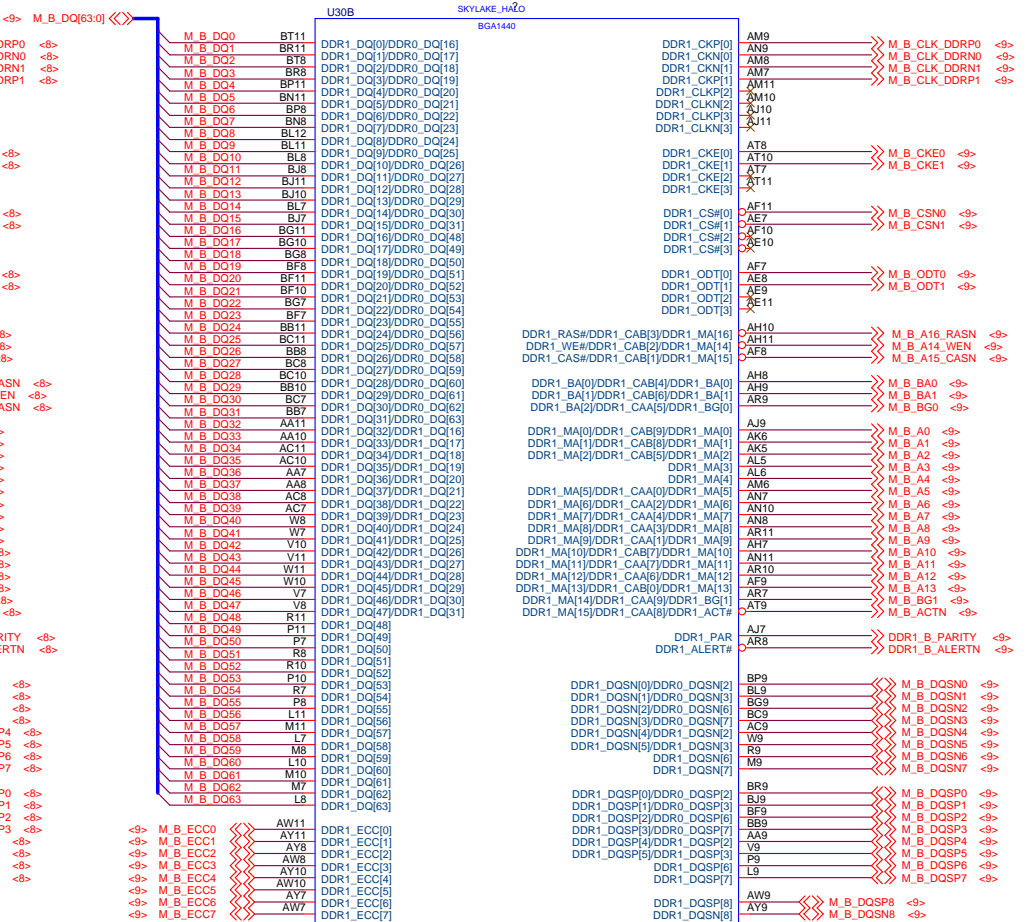
# Intel Kabylake Platform

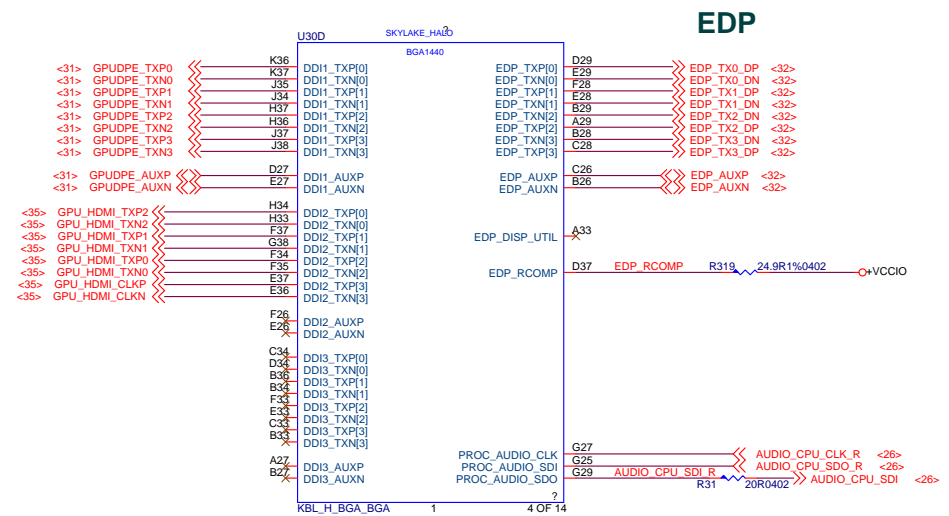
Page 01: Block Diagram  
 Page 02: Kabylake(HOST)  
 Page 03: Kabylake(DDR4)  
 Page 04: Kabylake(DMI/DISPLAY)  
 Page 05: Kabylake(Power)  
 Page 06: Kabylake(Power)  
 Page 07: Kabylake(Power)  
 Page 08: DDR4 SODIMM A0  
 Page 09: DDR4 SODIMM B0  
 Page 10: DGPU\_PCI-E Host  
 Page 11: DGPU\_MEM IF A/B  
 Page 12: DGPU\_GDDR5 FrameBuffer A0  
 Page 13: DGPU\_GDDR5 FrameBuffer A1  
 Page 14: DGPU\_GDDR5 FrameBuffer B0  
 Page 15: DGPU\_GDDR5 FrameBuffer B1  
 Page 16: DGPU\_POWER  
 Page 17: DGPU\_GND  
 Page 18: DGPU\_GPU DECOUPLING  
 Page 19: DGPU\_DACA,Display IF,XTAL  
 Page 20: DGPU\_ROM,H/W Straps  
 Page 21: DGPU\_GPIO,I2C  
 Page 22: DGPU\_Power Sequence  
 Page 23: DGPU\_Power Control/Discharge  
 Page 24: PCH-1 (CLK/DDI)  
 Page 25: PCH-2 (USB/SATA/PCIE)  
 Page 26: PCH-3 (HDA/RTC/SMBUS)  
 Page 27: PCH-4 (SPI/GPIO)  
 Page 28: PCH-5 (Power)  
 Page 29: LED 8051/KB CON  
 Page 30: EC(ENE9028)  
 Page 31: DP/USB3.0  
 Page 32: eDP/Camera  
 Page 33: ASM1142  
 Page 34: USB3.1 Type-C  
 Page 35: HDMI  
 Page 36: FAN/BTB,PWR,LED CONN  
 Page 37: M2 SSD/HDD/TPM  
 Page 38: GIGA\_LAN/WLAN/Touch Pad  
 Page 39: Audio CODEC/Audio AMP/MIC  
 Page 40: Speaker  
 Page 41: Woofer  
 Page 42: Battery Select/Charger  
 Page 43: System Power/3V LCD  
 Page 44: +1.2VDIMM/+0.6VRUN/+2.5VMEM  
 Page 45: +1V/+PEX\_VDD/+1.24V/+1V8\_SUS  
 Page 46: CPU Power (ISL95855)  
 Page 47: CPU1(VCore/VCCGT)  
 Page 48: CPU2(VCCSA/VCCIO)  
 Page 49: DGPU POWER FBVDDQ  
 Page 50: DGPU POWER NVVDD1  
 Page 51: DGPU POWER NVVDD2  
 Page 52: DGPU POWER NVVDD3  
 Page 53: EMI/Screw/ME  
 Page 54: Power Delivery Chart  
 Page 55: Power on Sequence  
 Page 56: Power down Sequence  
 Page 57: Power on Block Diagram  
 Page 58: History  
 Page 59: [A]LED/Touch Pad  
 Page 60: [B]Card reader/BTB CONN  
 Page 61: [B]USB3.0  
 Page 62: [D]Power Switch  
 Page 63: TOP  
 Page 64: BOTTOM

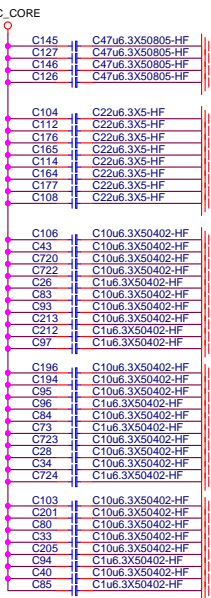
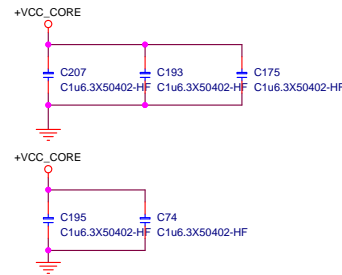
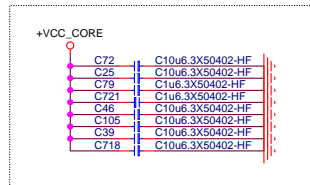
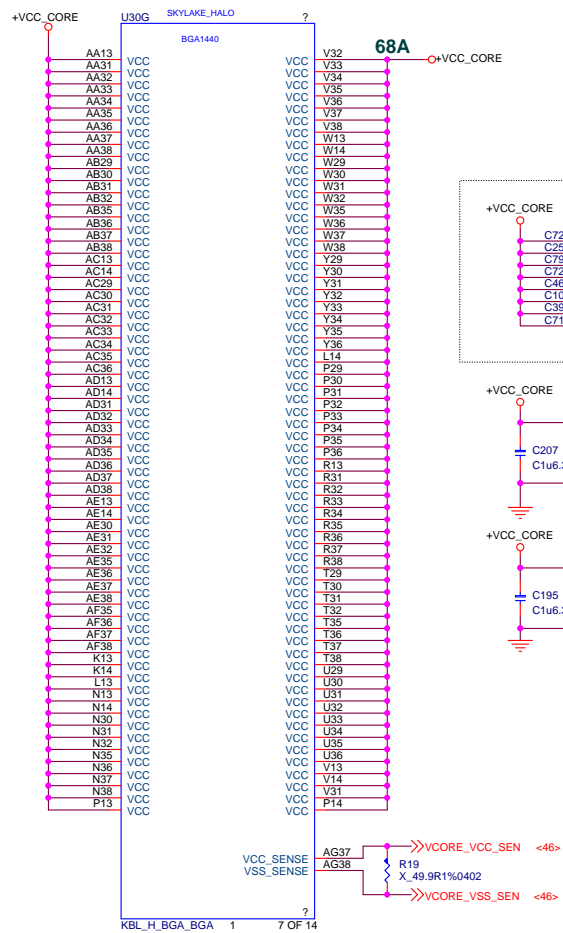




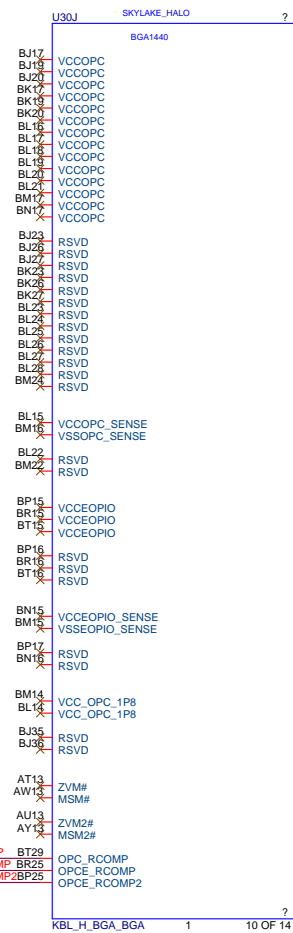
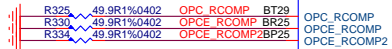
## DDR Channel B

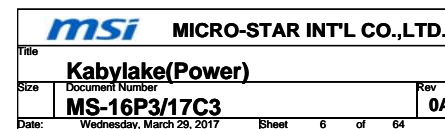
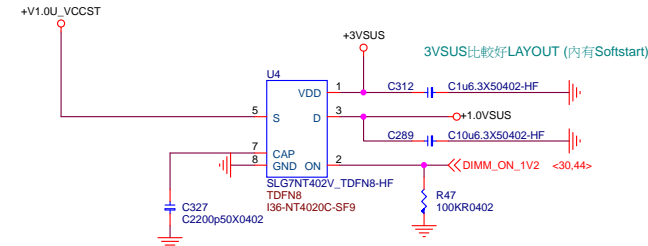




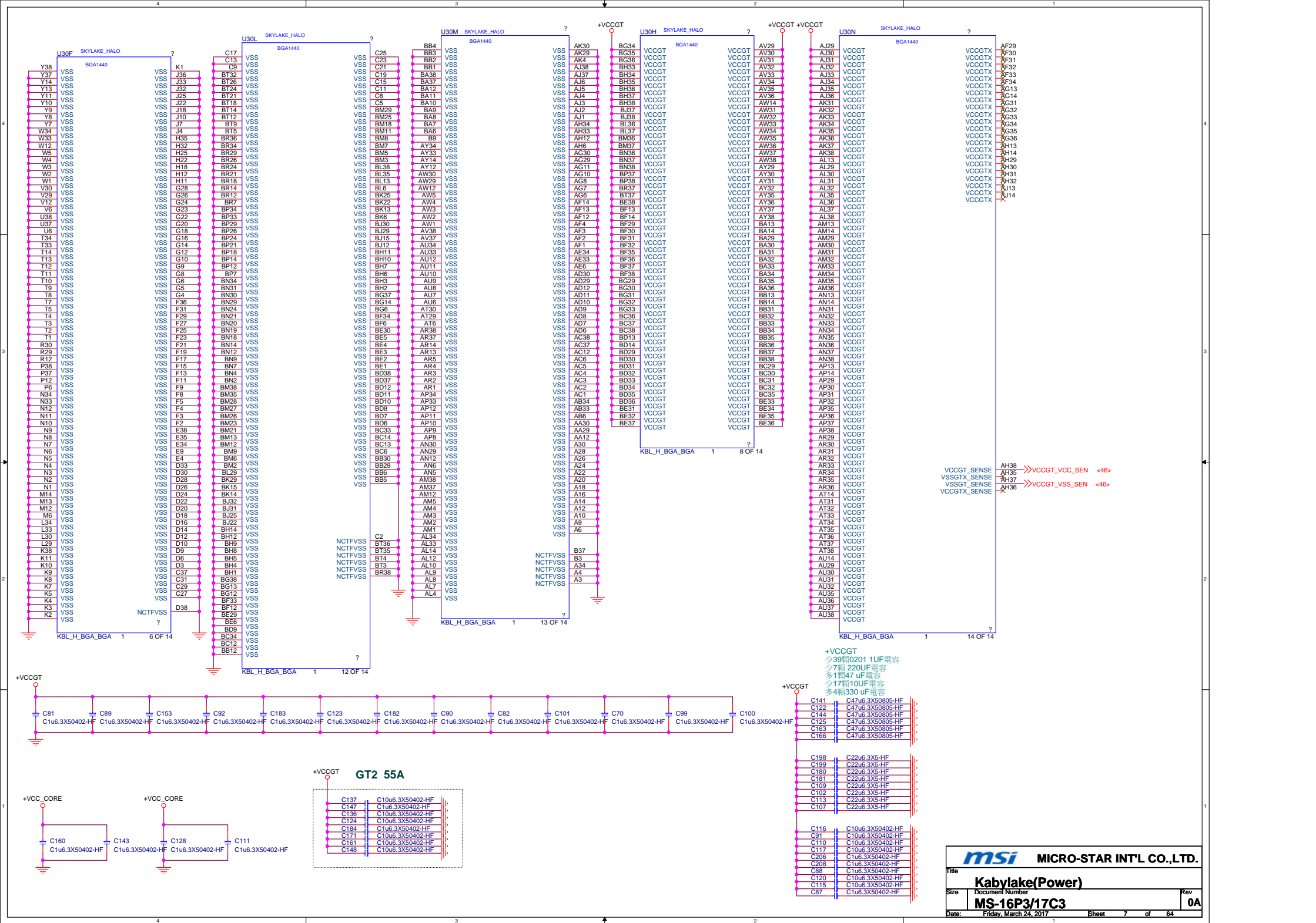


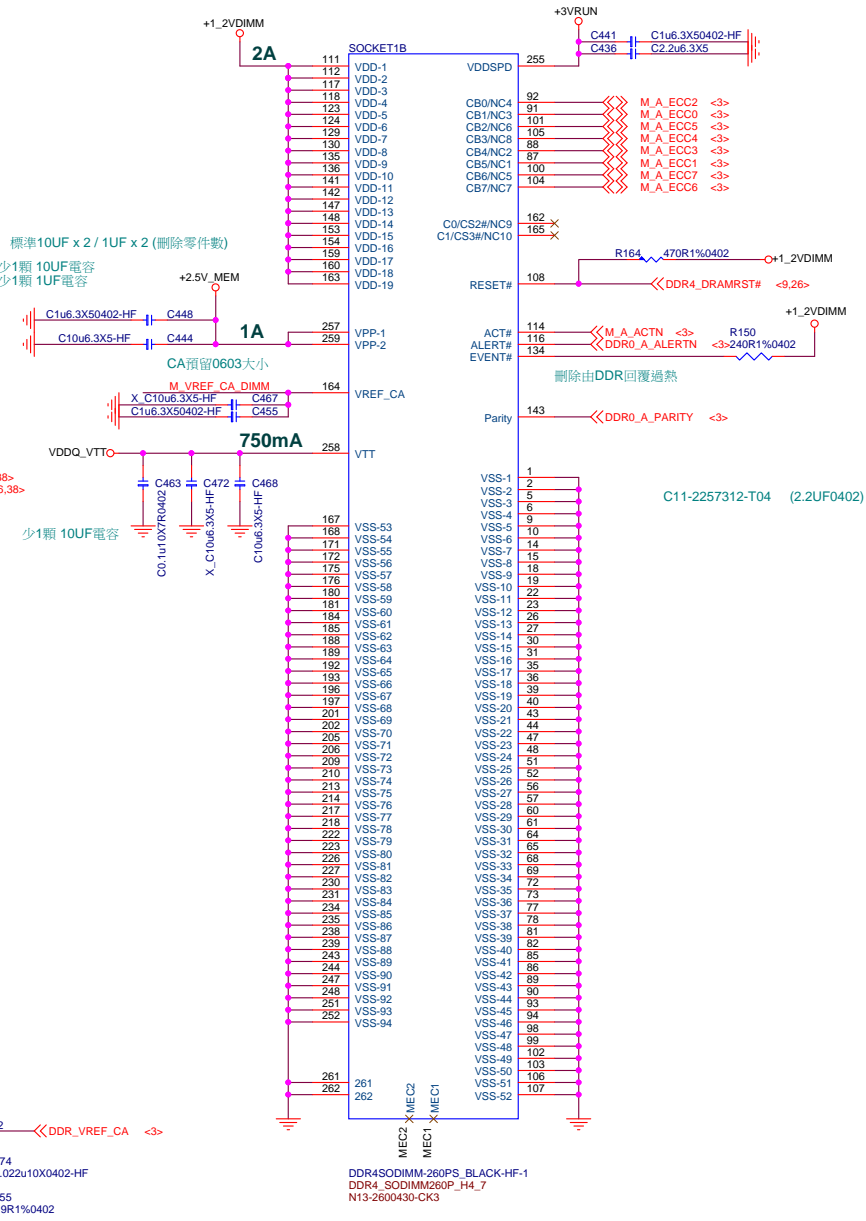
少31顆0201 1uF電容  
少5顆 220uF電容  
多8顆10 uF電容  
多4顆330 uF電容





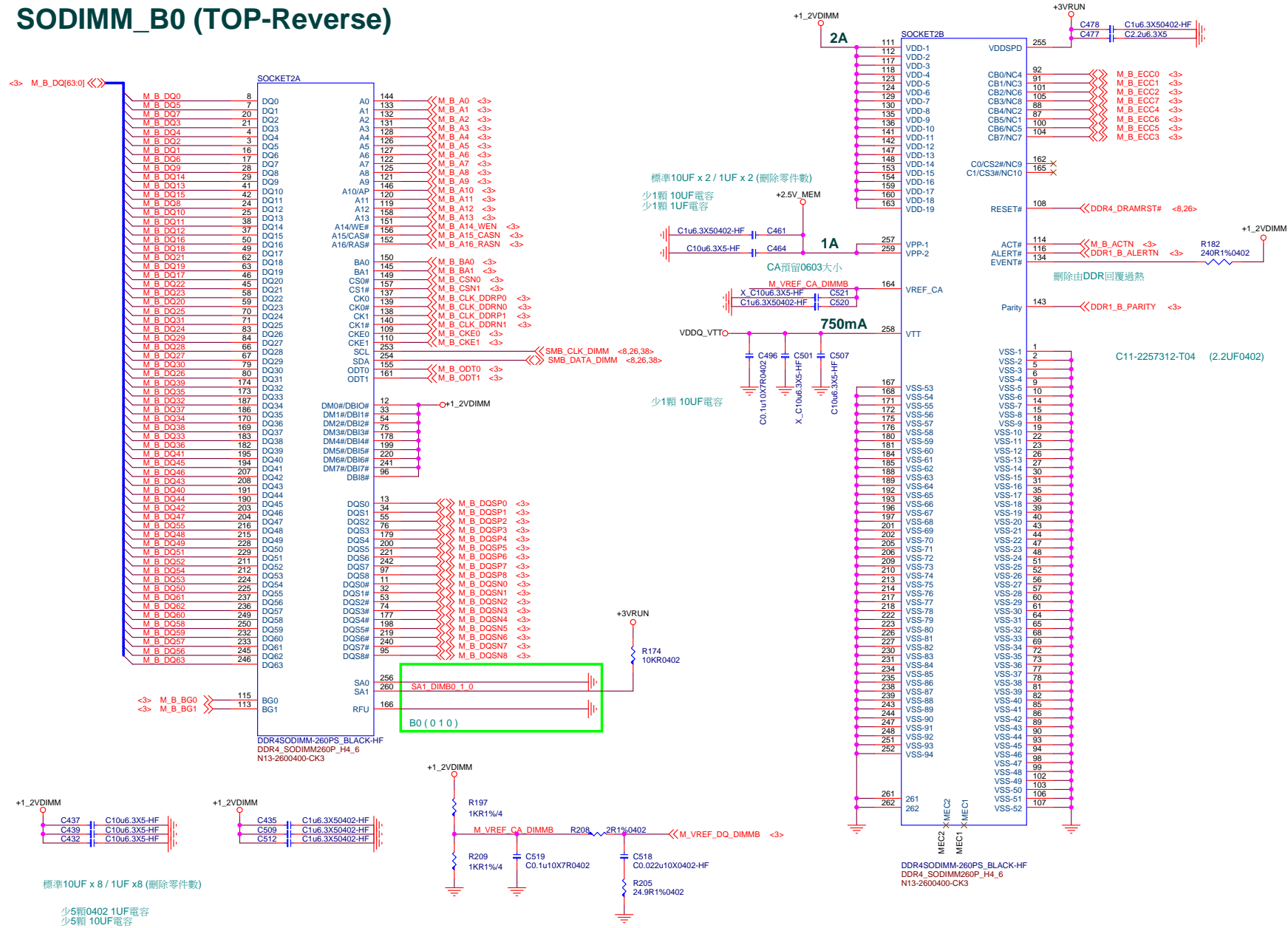




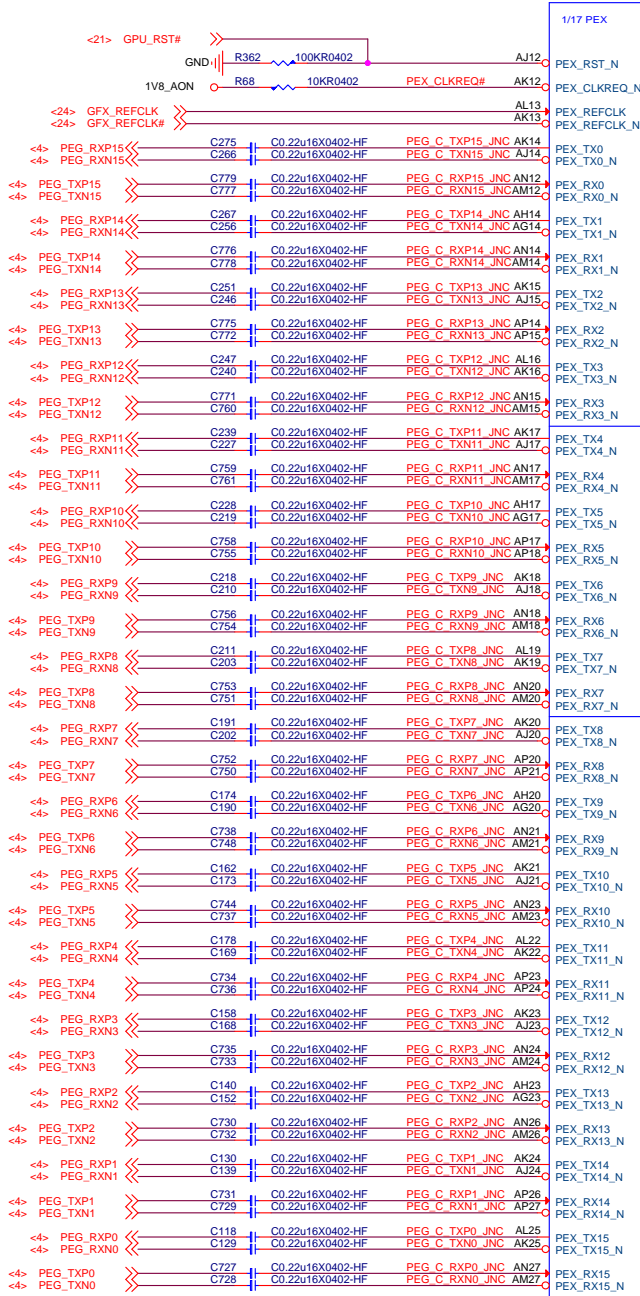
[illegible]



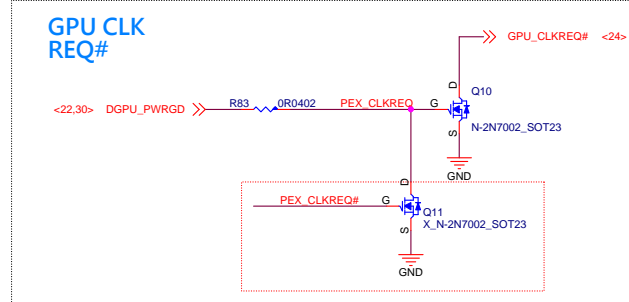
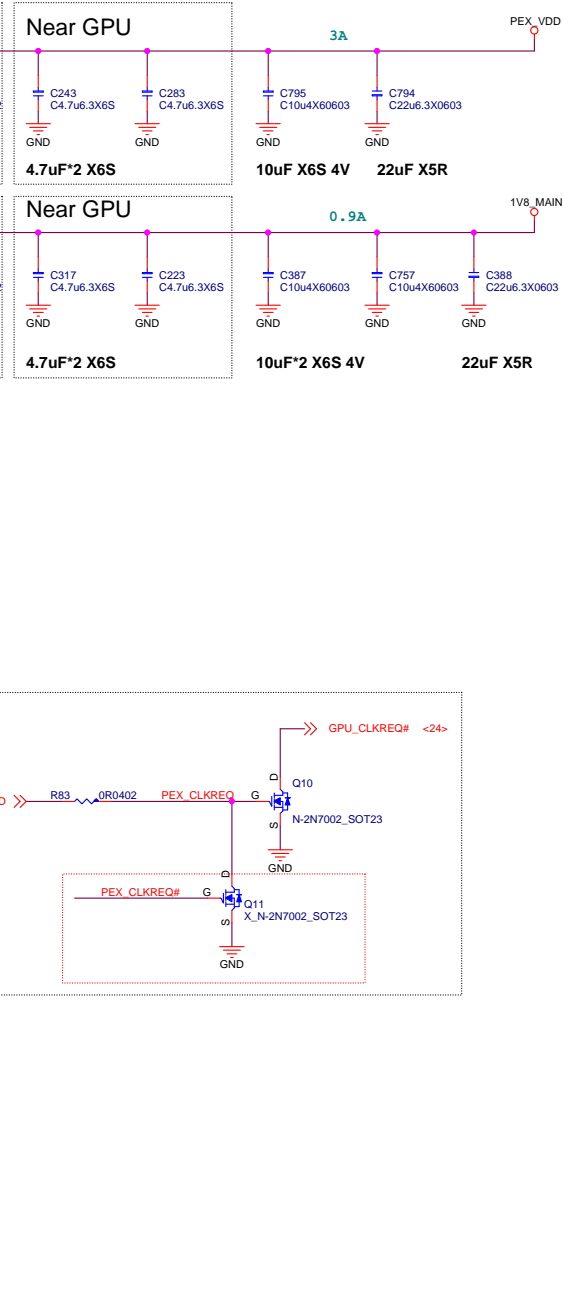
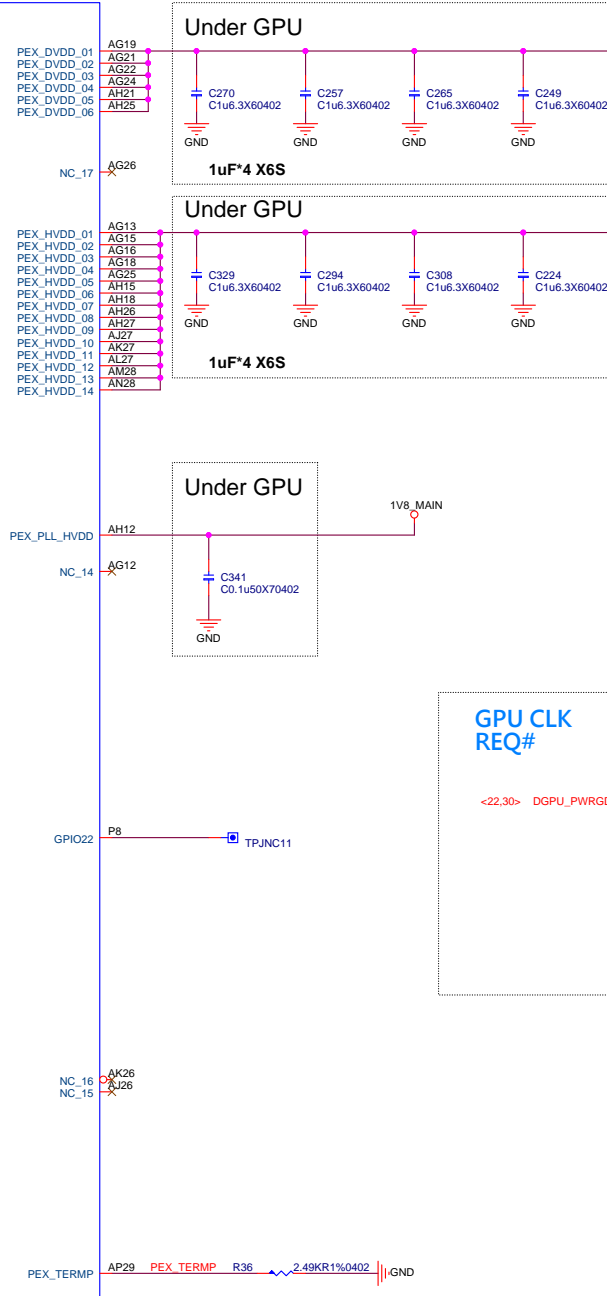
# SODIMM\_B0 (TOP-Reverse)



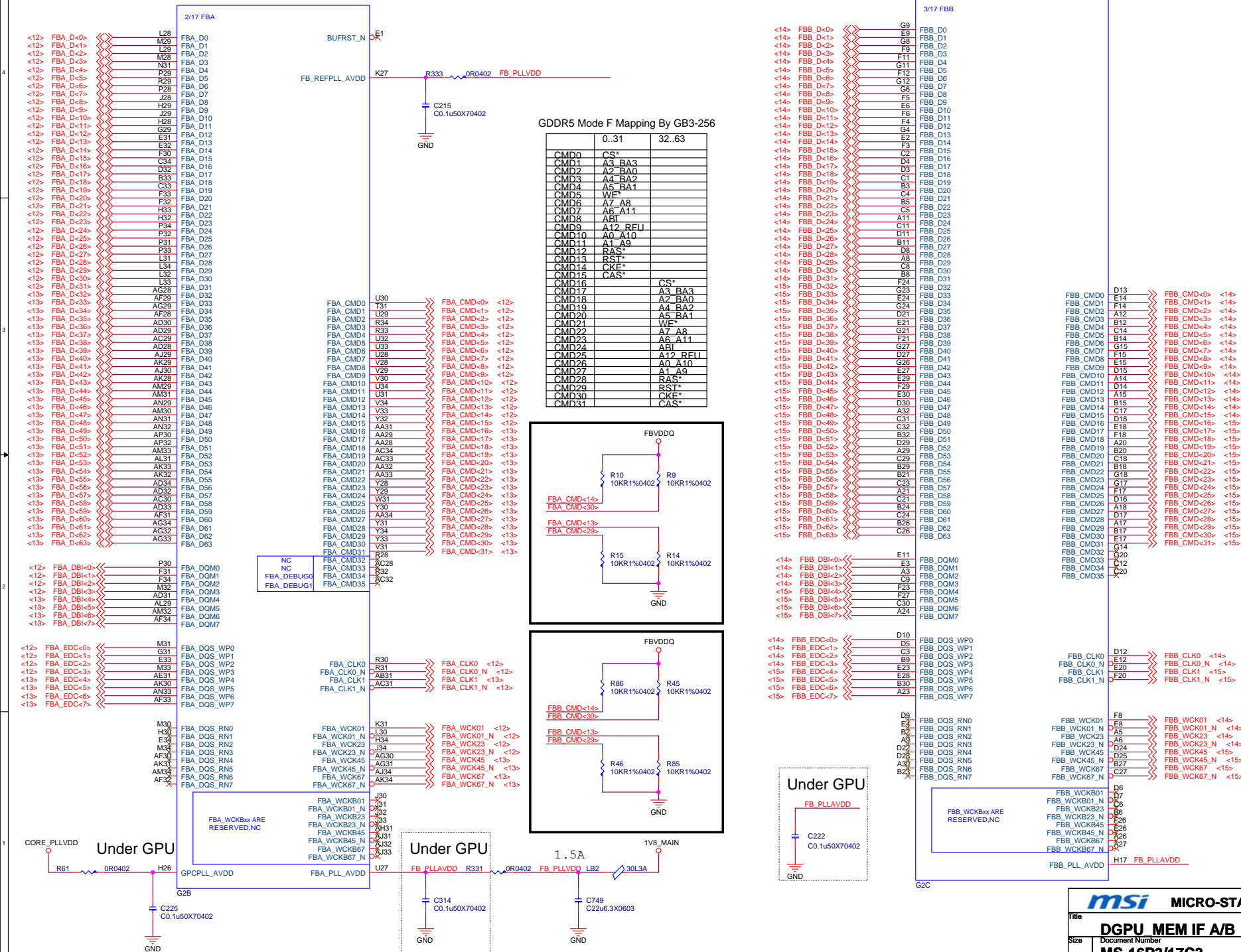
# GPU PCI EXPRESS



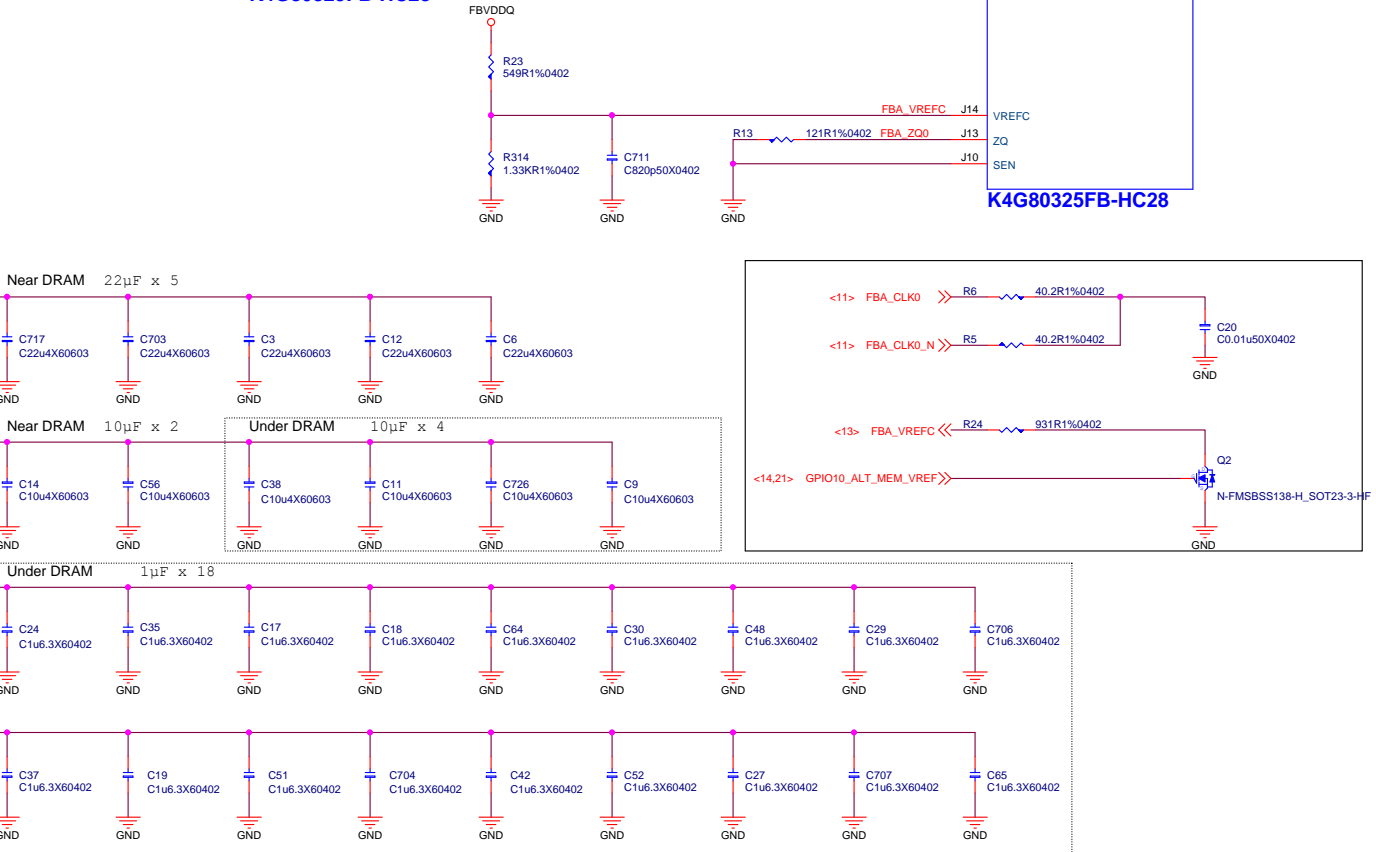
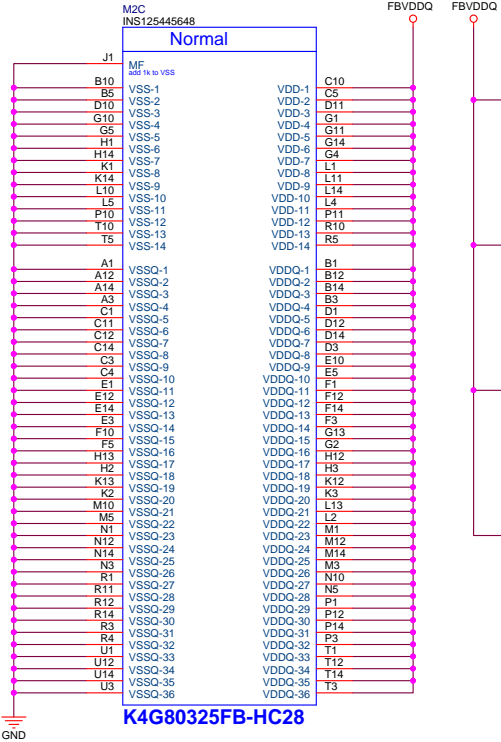
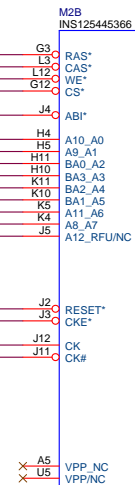
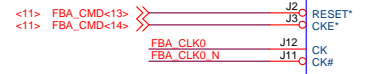
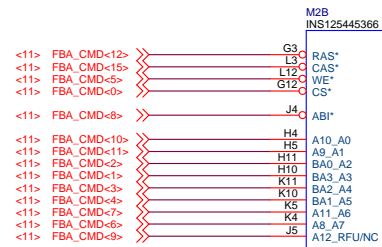
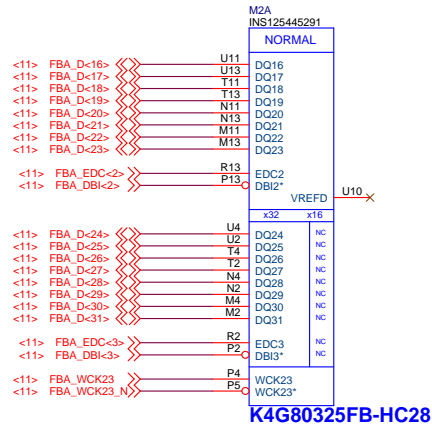
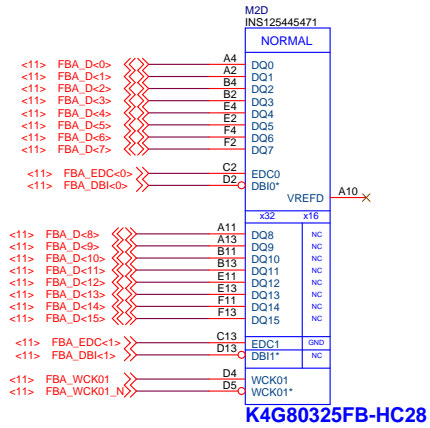
PEX LANES 4 TO 15 NC FOR GM108  
PEX LANES 0 TO 3 NC FOR GM117



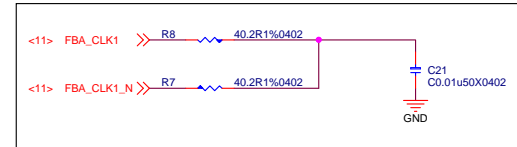
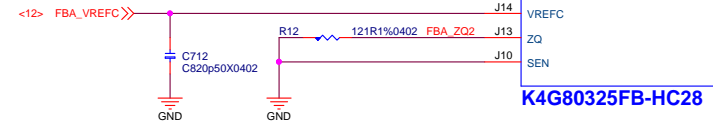
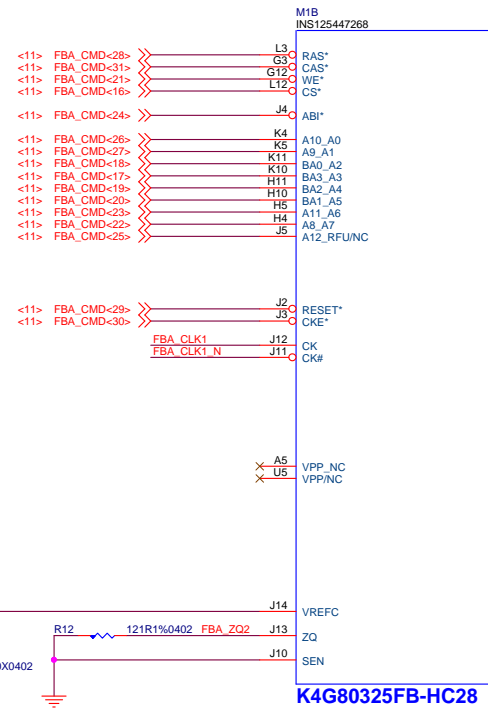
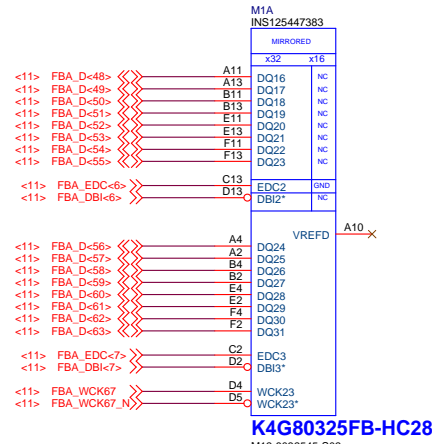
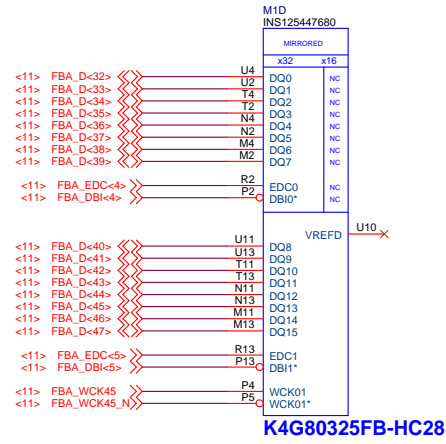
## GPU Frame Buffer Partition A/B



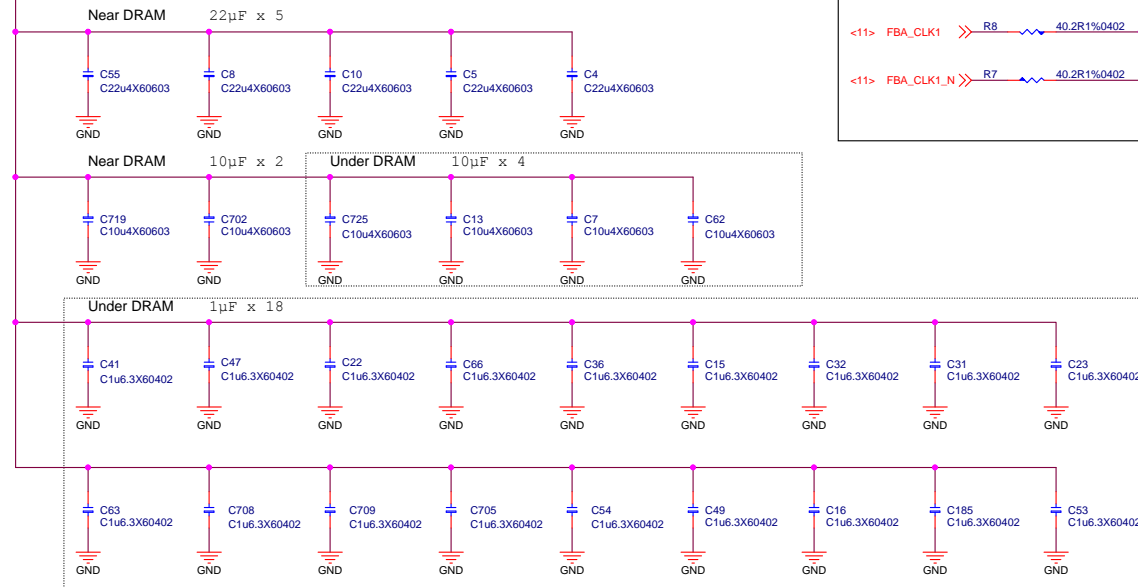
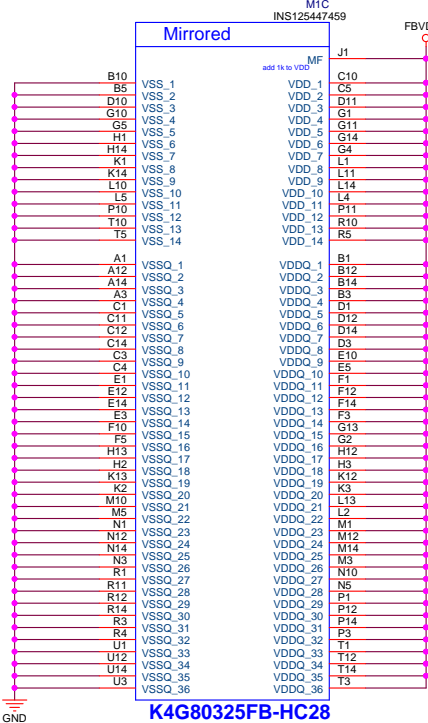
## DGPU\_GDDR5 FrameBuffer A0



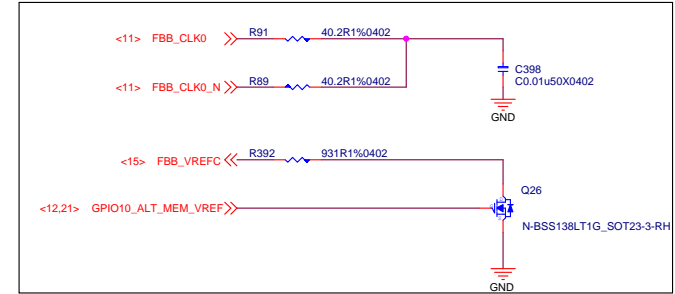
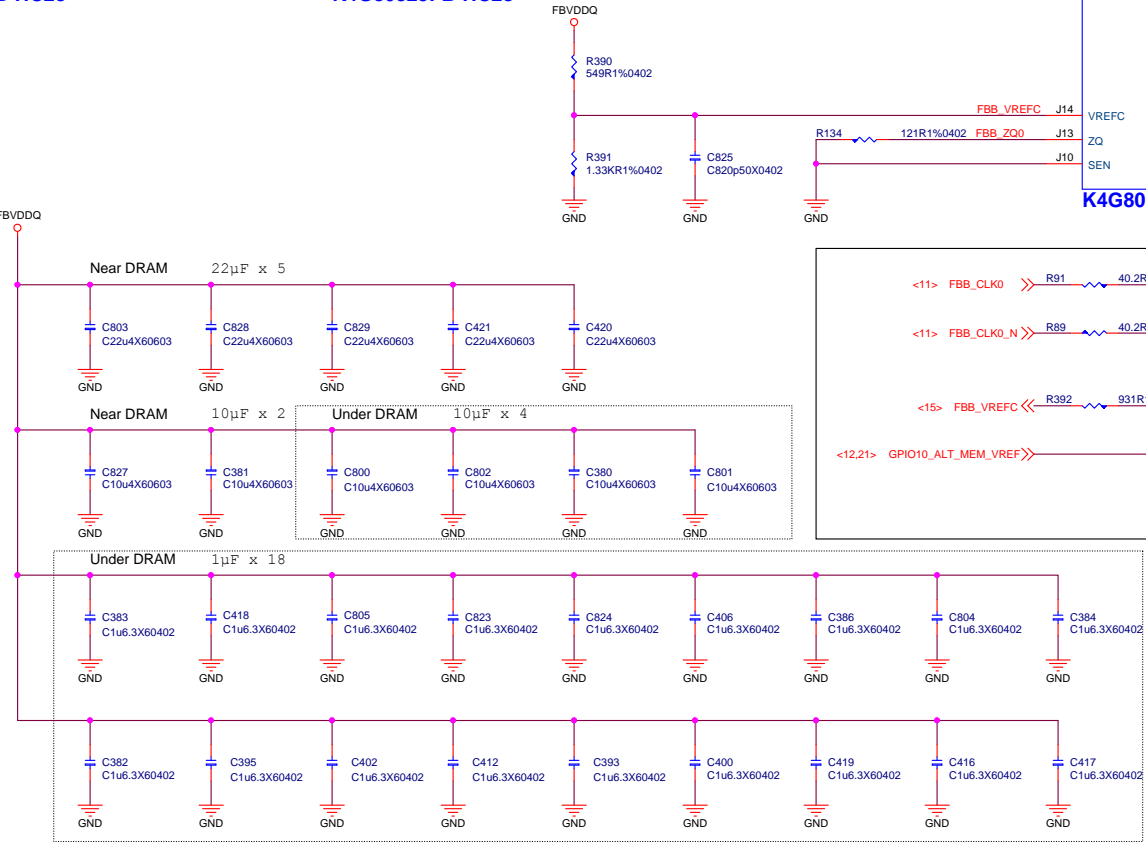
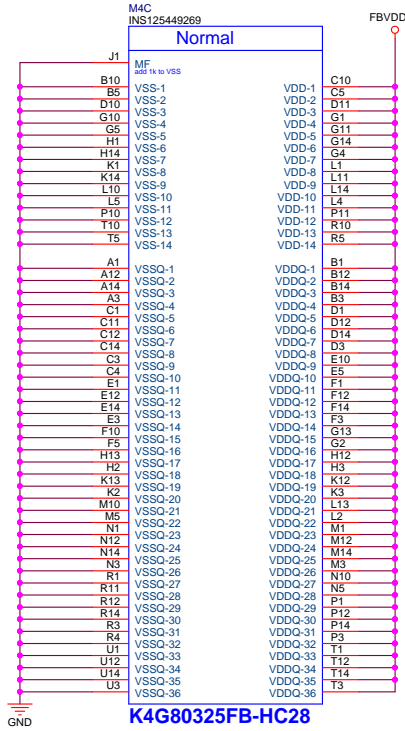
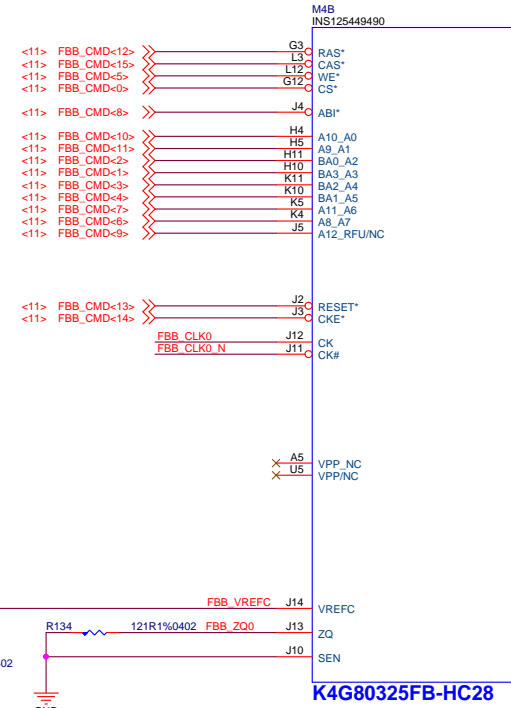
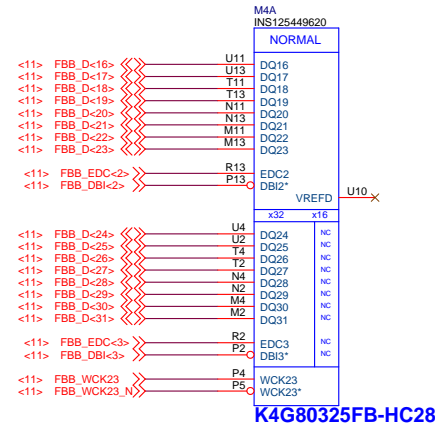
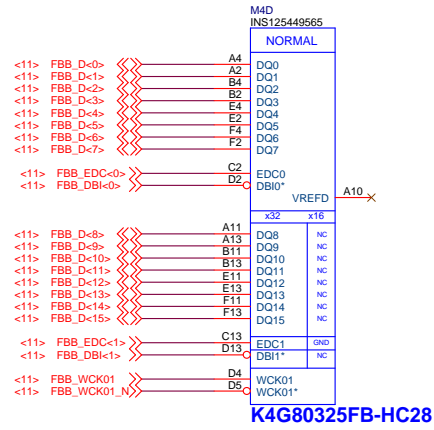
# DGPU\_GDDR5 FrameBuffer A1



2016/03/23 Remove R14 to follow NV CRB

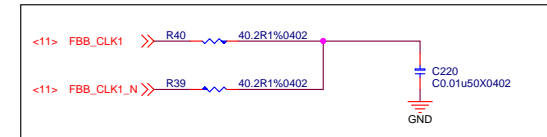
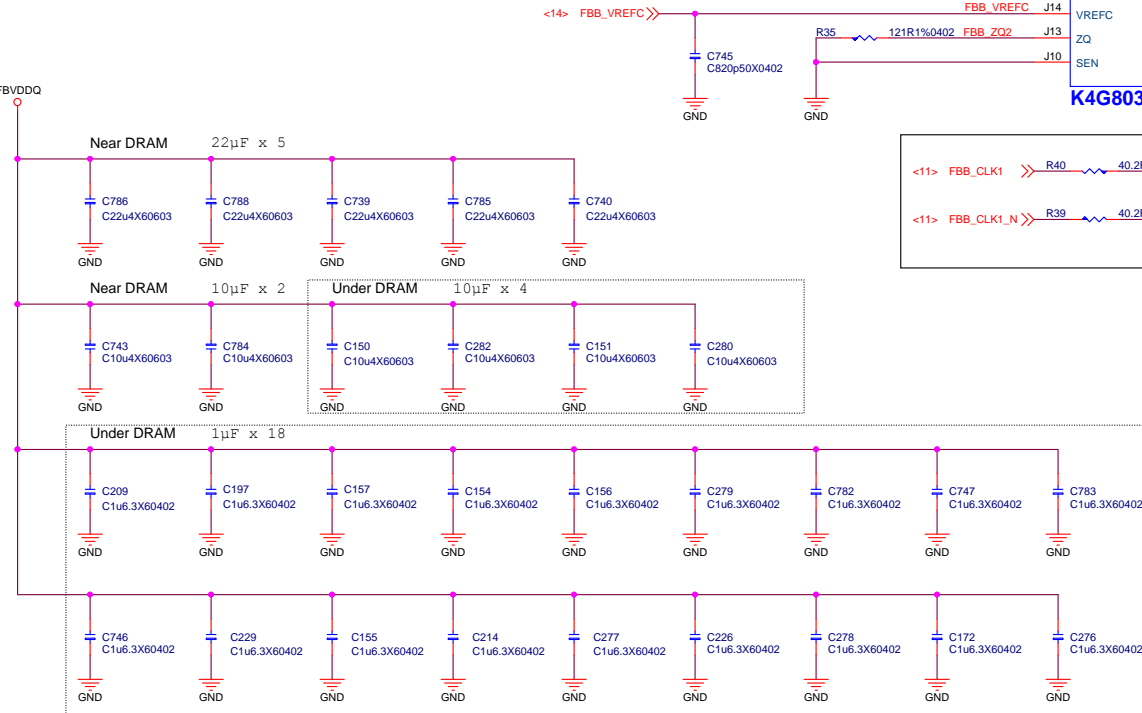
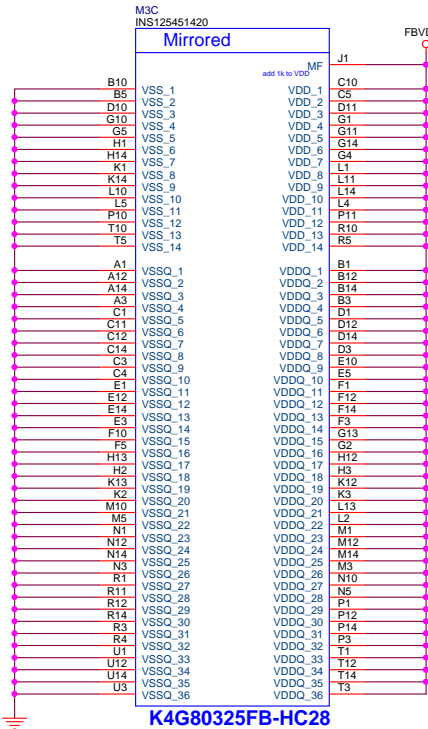
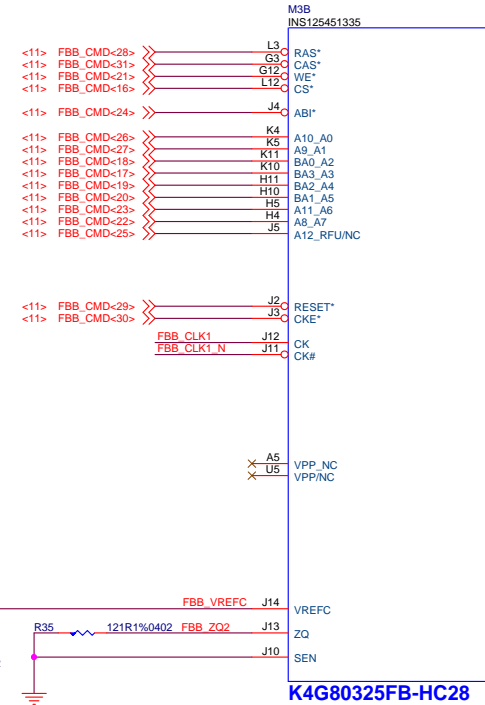
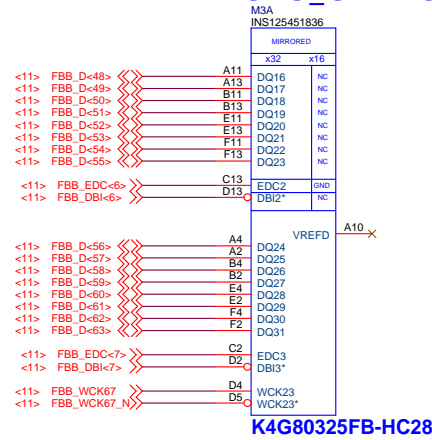
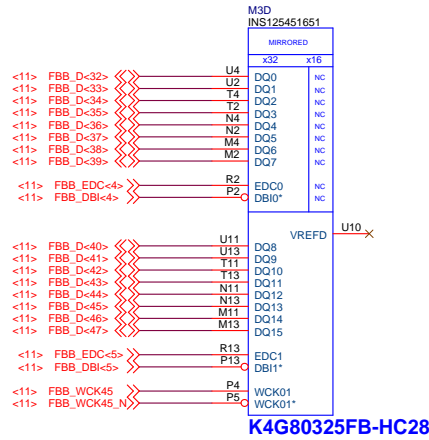


# DGPU\_GDDR5 FrameBuffer B0

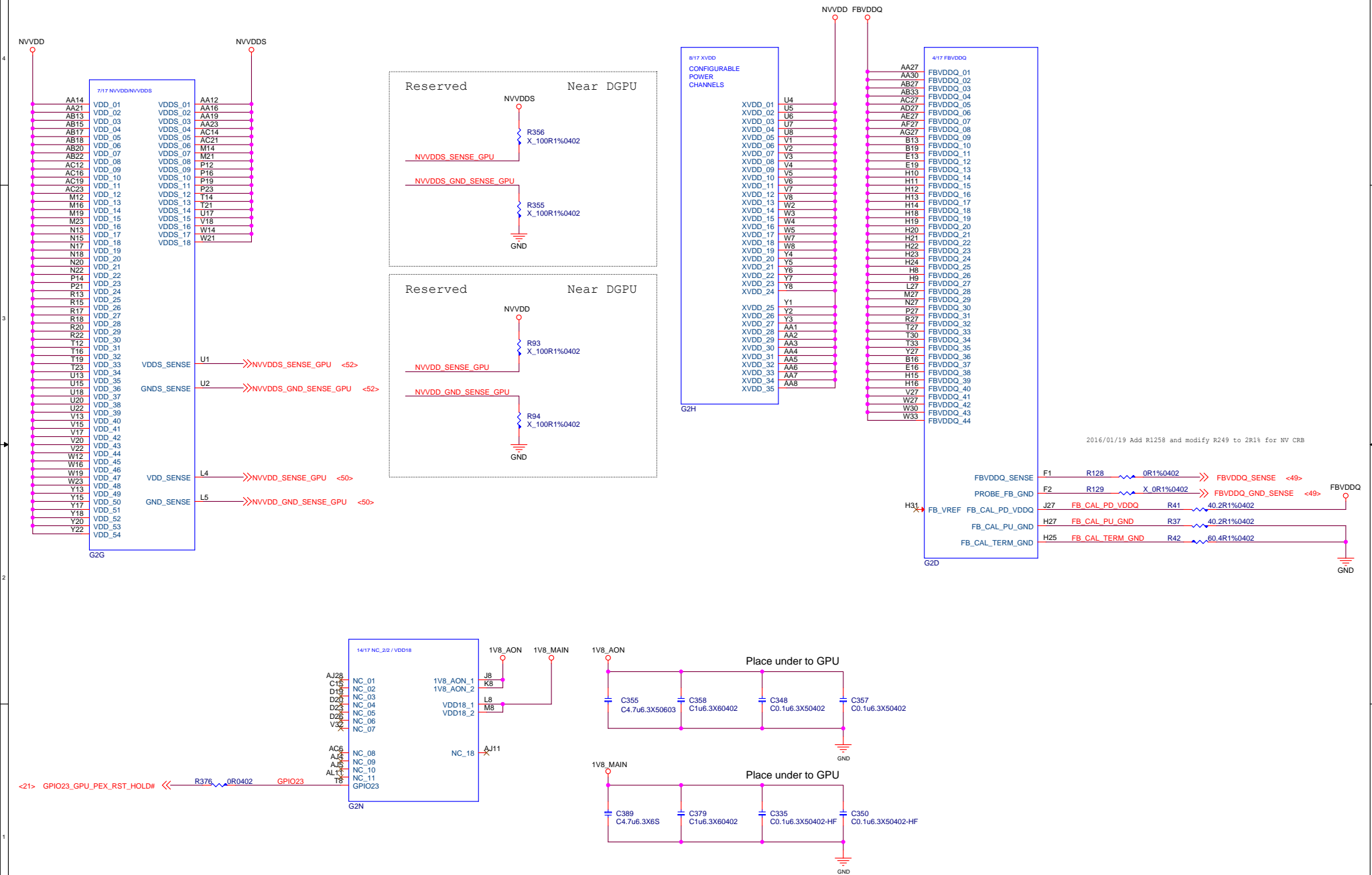




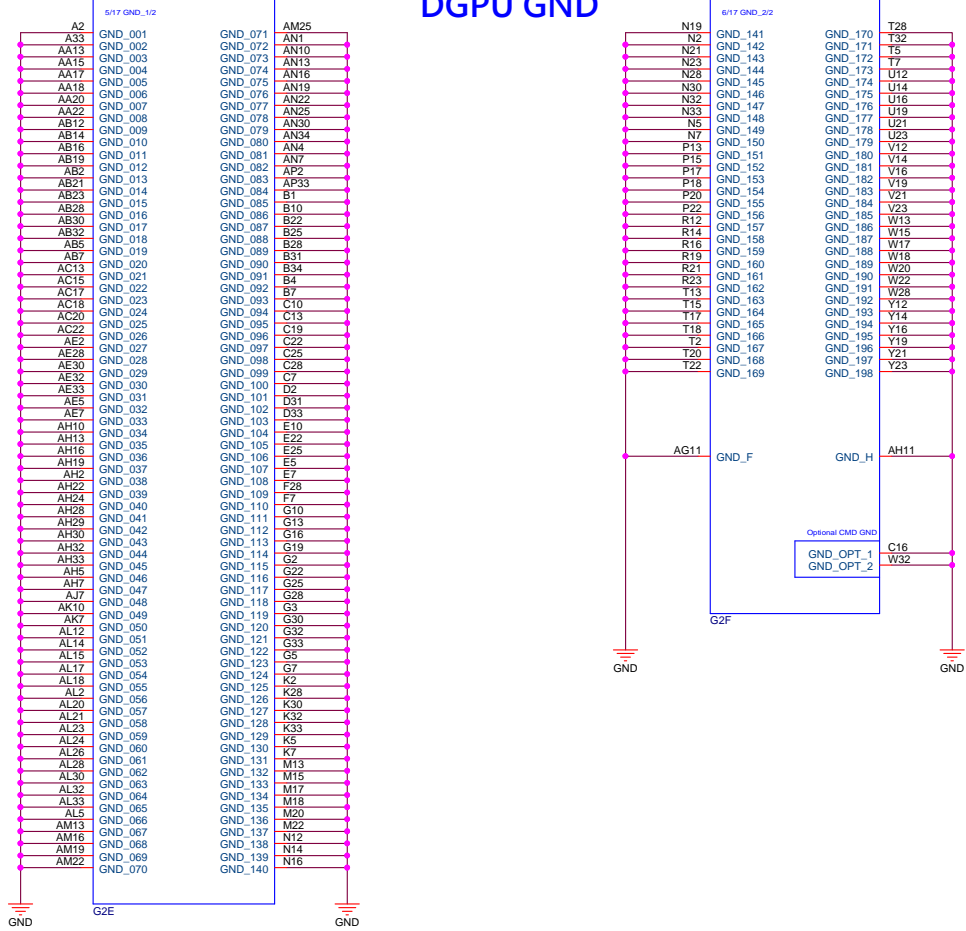
# DGPU\_GDDR5 FrameBuffer B1



# GPU NVVDD, FBVDDQ



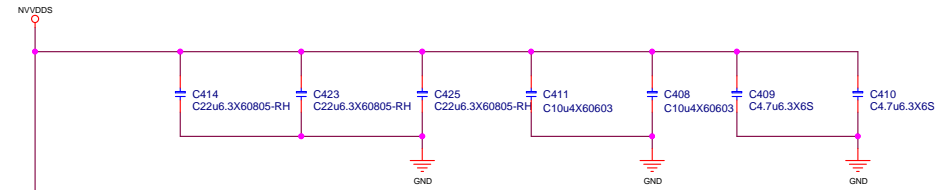
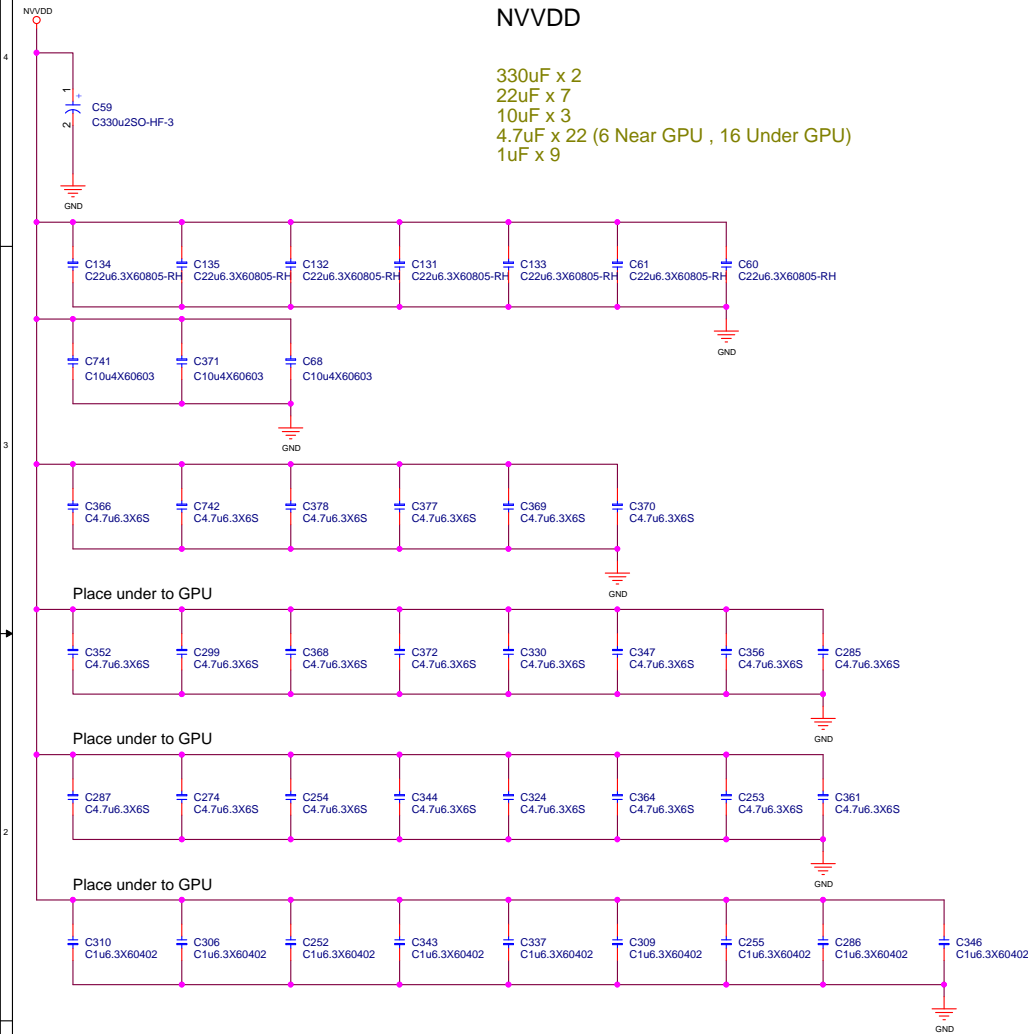
DGPU GND



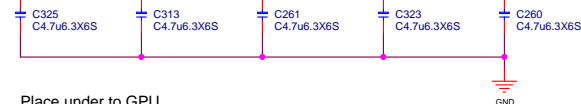
# GPU DECOUPLING

## NVVD

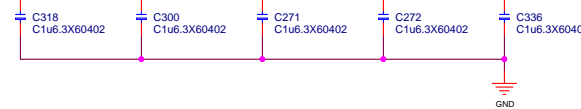
330uF x 2  
22uF x 7  
10uF x 3  
4.7uF x 22 (6 Near GPU , 16 Under GPU)  
1uF x 9



Place under to GPU



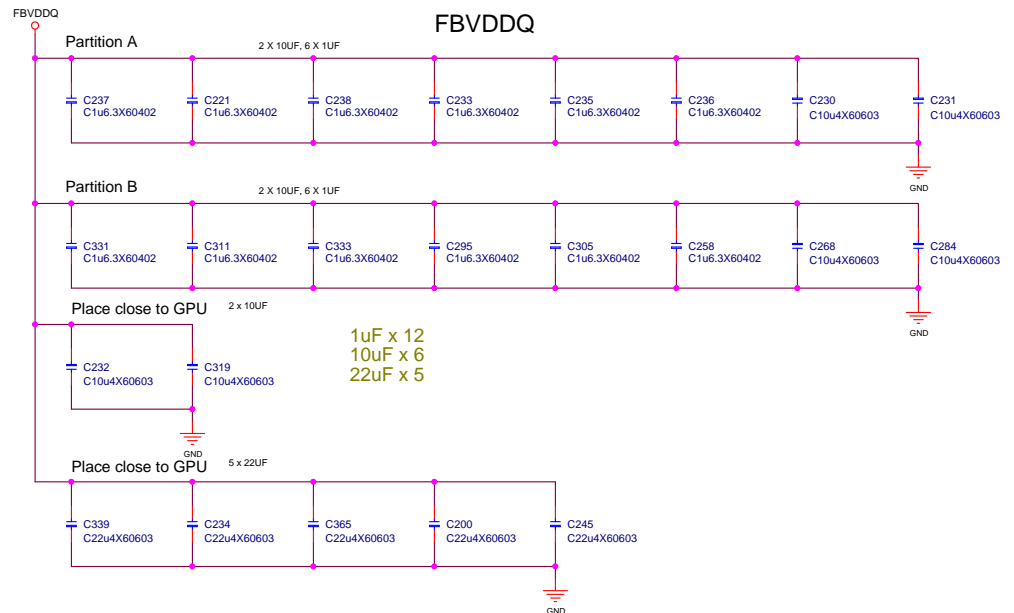
Place under to GPU



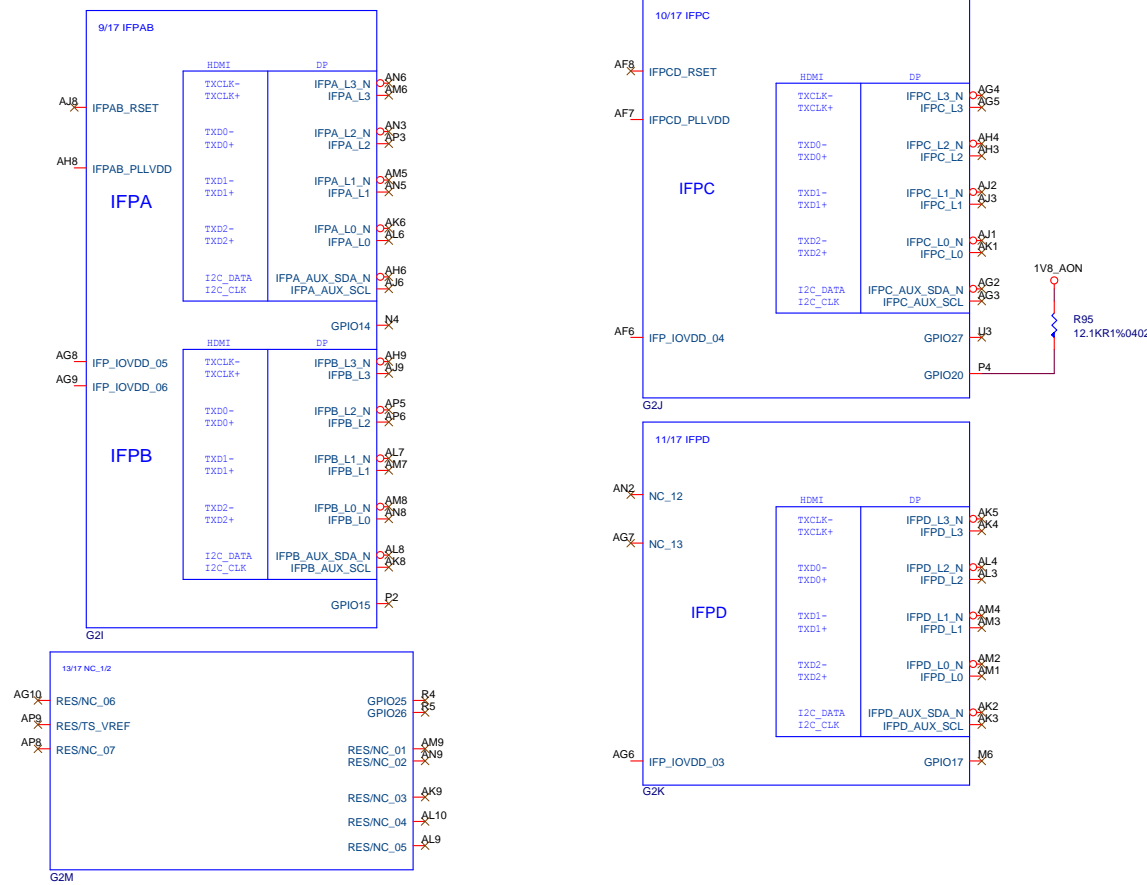
## NVVDS

330uF x 1  
22uF x 3  
10uF x 2  
4.7uF x 7 (2 Near GPU , 5 Under GPU)  
1uF x 5

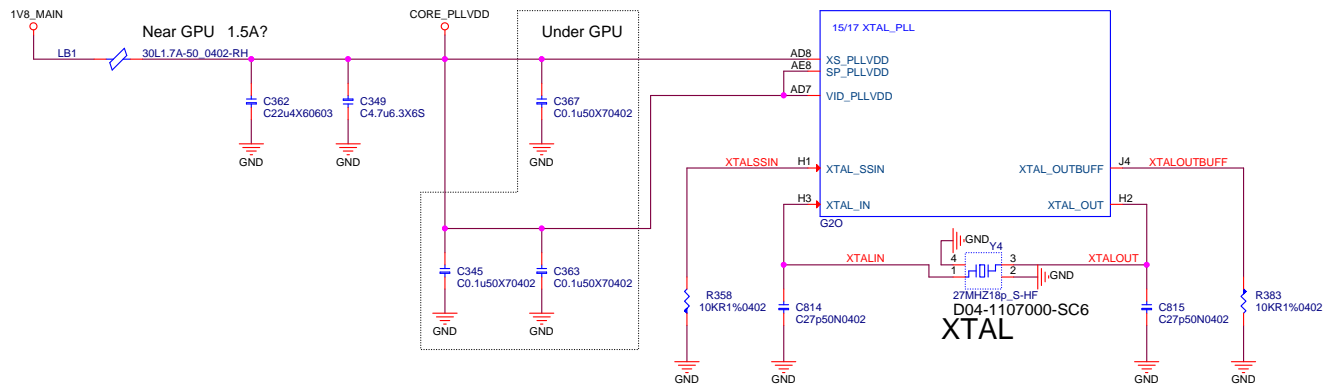
## FBVDDQ



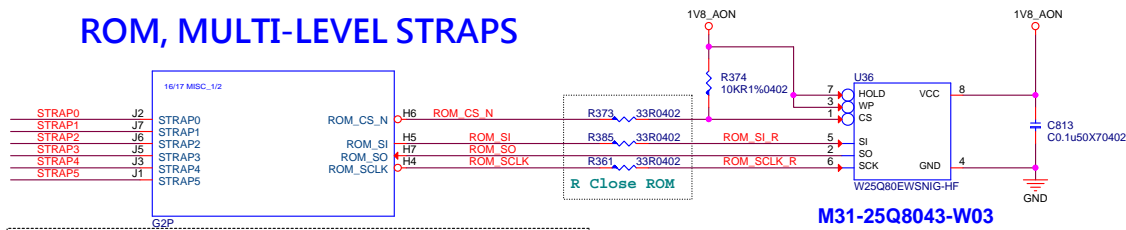
# DACA,Display IF



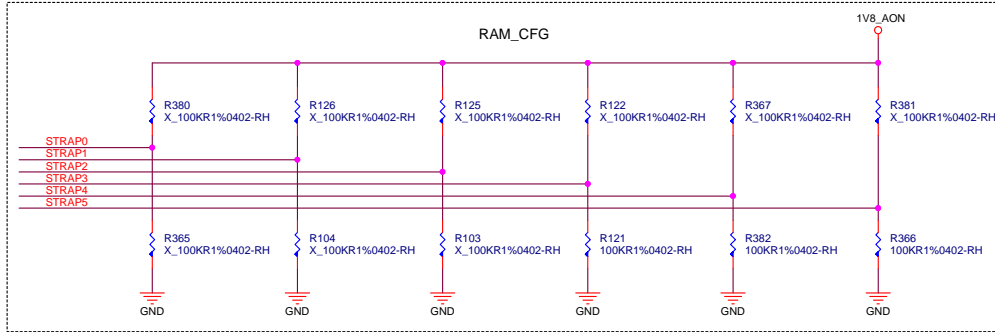
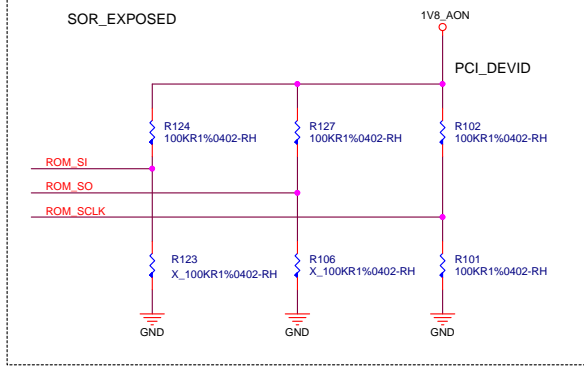
# DGPU XTAL



# ROM, MULTI-LEVEL STRAPS



M31-25Q8043-W03



STRAP2	STRAP1	STRAP0	RAMCFG[4:0]	STRAP Set
L	L	L	0x0 Samsung: M12-8032545-S02 / K4G80325FB-HC28	R330.R92.R91
L	L	H	0x1 Micron: MT51J256M32HF-70:A	R354.R92.R91
L	H	L	0x2 Hynix: M12-5GC8H05-H23 / H5GC8H24MJR-R0C	R330.R106.R91
L	H	H		
H	L	L		
H	L	H		
H	H	L	0x6 Hynix: M12-5GC4HG5-H23 / H5GC4H24AJR-R0C	R330.R106.R105
H	H	H	0x7 Samsung: M12-41325A5-S02 / K4G41325FE-HC28	R354.R106.R105
L	L	M	0x8 Micron: EDW032BABG-70:F:A	R330.R354.R92.R91
L	M	L		

H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

1:SMB\_ALT\_ADDR ENABLE  
0:SMB\_ALT\_ADDR DISABLE  
  
1:DEVID\_SEL REBRAND  
0:DEVID\_SEL ORIGINAL  
  
1:PCIE\_CFG LOW POWER  
0:PCIE\_CFG HIGH POWER  
  
1:VGA\_DEVICE ENABLE  
0:VGA\_DEVICE DISABLE  
  
H=High :Tied to 1.8V  
M=Middle:Tied to 0.9V  
L=Low :Tied to 0V

ROM\_SO ROM\_SI ROM\_SCLK SOR\_EXPOSED[3:0] 1:ENABLE 0:DISABLE

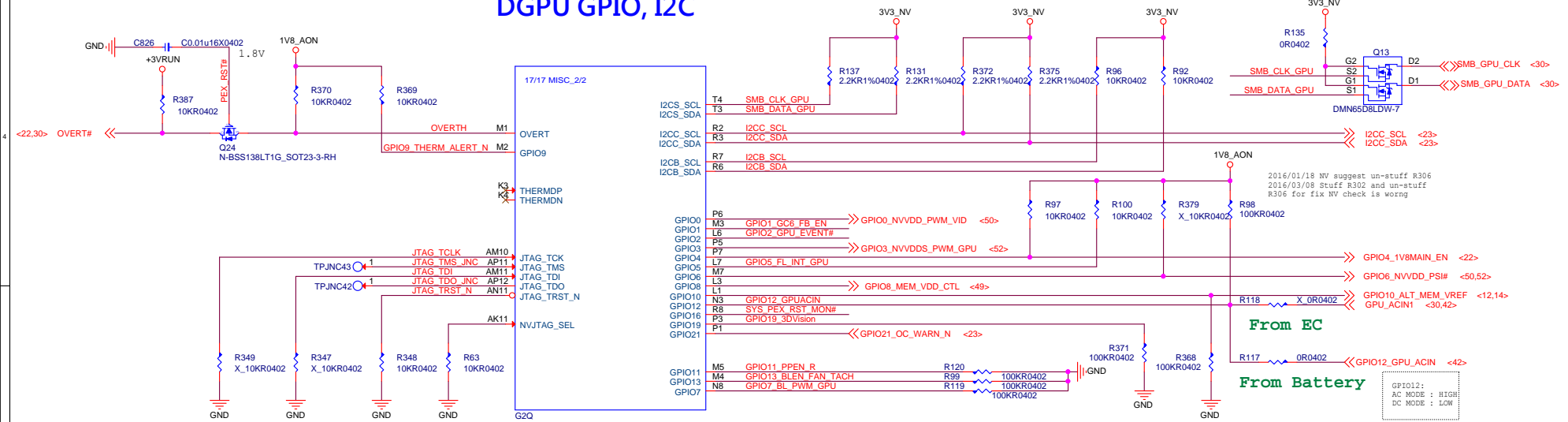
L	L	L	1111	DEFAULT	SOR0/1/2/3 ENABLE
L	L	H	1110		
L	H	L	1101		
L	H	H	1100		
H	L	L	1011		
H	L	H	1010		
H	H	L	1001		
H	H	H	1000		
L	L	M	0111		
L	M	L	0110		
L	M	H	0101		
L	H	M	0100		
H	L	M	0011		
H	M	L	0010		
H	M	H	0001		
H	H	M	0000		V

STRAP5 STRAP4 STRAP3 SMB\_ALT\_ADDR DEVID\_SEL PCIE\_CFG VGA\_DEVICE

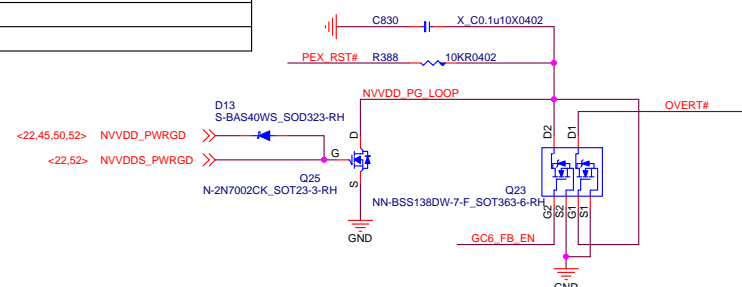
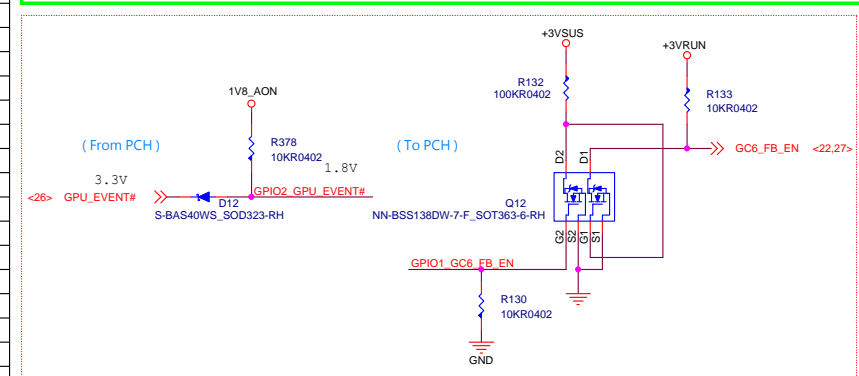
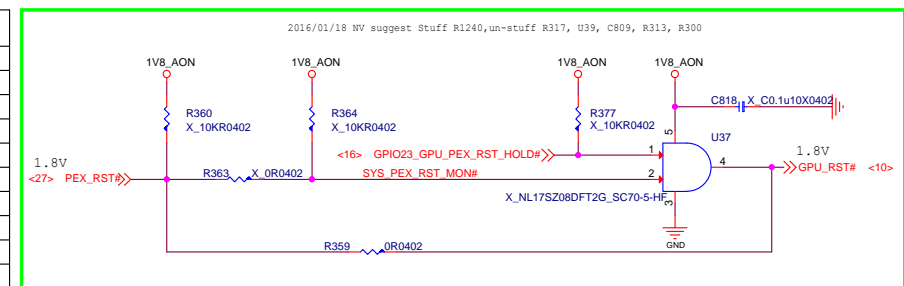
M	H	H	1	1	1	1
M	H	L	1	1	1	0
M	L	H	1	1	0	1
M	L	L	1	1	0	0
L	H	M	1	0	1	1
L	M	H	1	0	1	0
L	M	L	1	0	0	1
L	L	M	1	0	0	0
H	H	H	0	1	1	1
H	H	L	0	1	1	0
H	L	H	0	1	0	1
H	L	L	0	1	0	0
L	H	H	0	0	1	1
L	H	L	0	0	1	0
L	L	H	0	0	0	1 DEFAULT
L	L	L	0	0	0	0 V



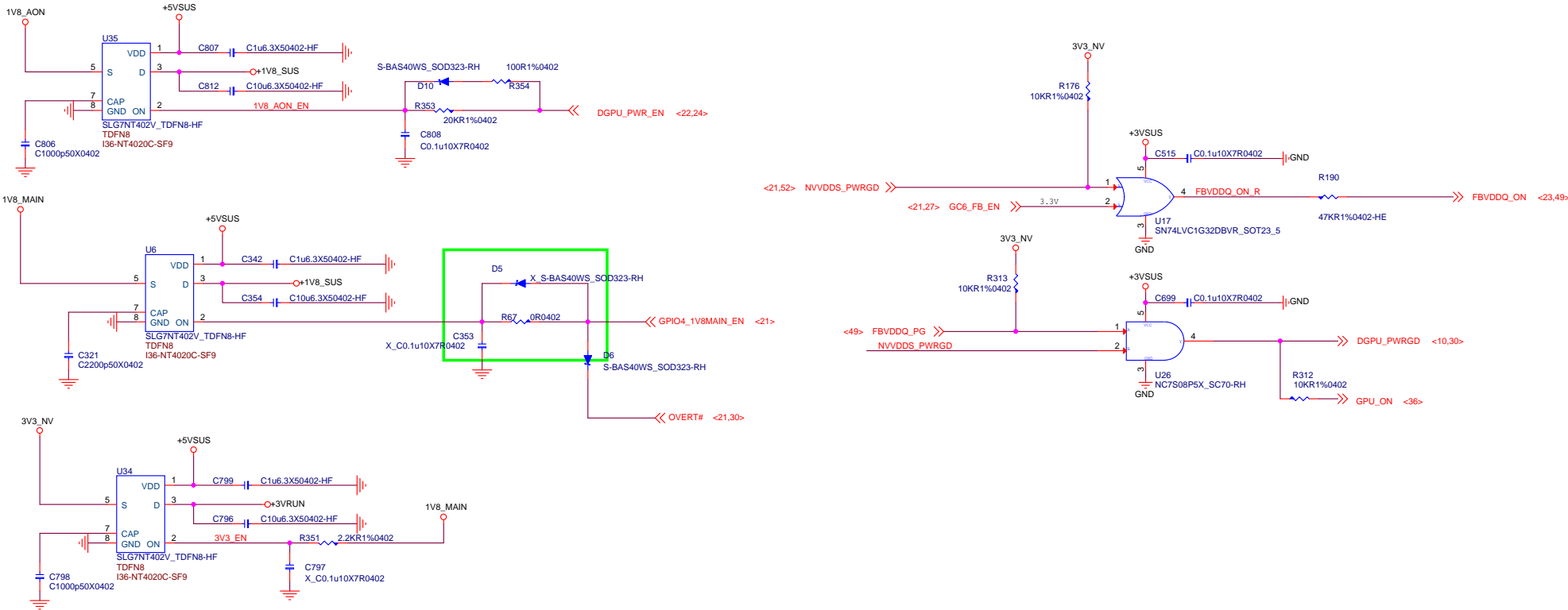
# DGPU GPIO, I2C



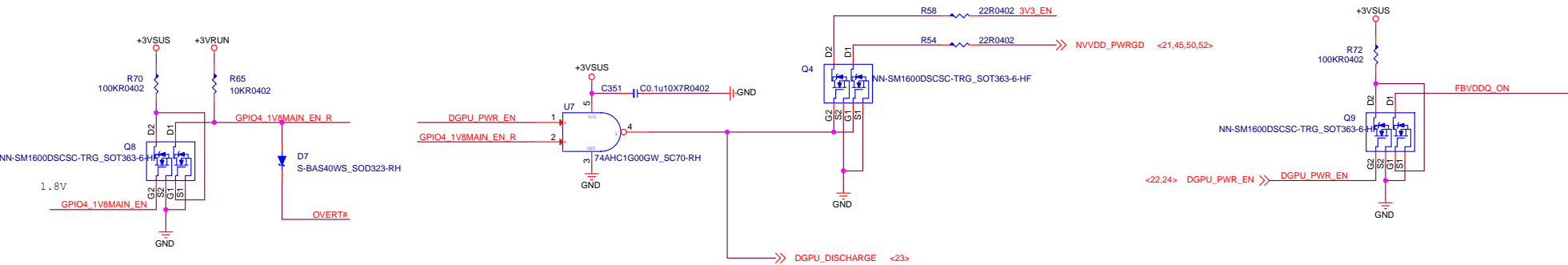
Pin Name	Normal function	I/O	Functional Description	Recommended Default Pull-up or Pull-down
GPIO0	PWR_VID	O	GPU Core VDD PWM control signal	0 to 1V8 PWM output
GPIO1	GC6_FB_EN	O	FB Enable for GC6 2.1	OD, 10K pull-down
GPIO2	GPU_EVENT#	I	GPU wake signal for GC6 2.1	10K pull-up to 1V8 _AON
GPIO3	NVVDD_SRAM_PWM	O	PWM output to control the SRAM power supply	0 to 1V8 output
GPIO4	1V8_MAIN_EN	O	GPU POWER Sequencing for GC6 2.1	OD, 10K pull-up to 1V8 _AON
GPIO5	FRM_LCK#	I	Active low Frame Lock	OD, 1V8 pull-up to 1V8 _AON
GPIO6	NVVDD_PSI	O	Phase shedding	10K pull-up to 1V8 _AON
GPIO7	LCD_BL_PWM	O	Panel Backlight PWM Brightness Control	100K pull-down
GPIO8	MEM_VDD_CTL	O	Memory Voltage Control	pull-up/pull-down to set the FBVDD/Q power-on voltage
GPIO9	THERM_ALERT	I/O	Active Low Thermal Alert	OD, 10K pull-up to 1V8 _AON
GPIO10	MEM_VREF_CTL	O	Memory VREF Control	100K pull-down
GPIO11	LCD_VCC	O	Panel Power Enable	100K pull-down
GPIO12	PWR_LEVEL	I	AC power detect or power supply overdraw input	100K pull-up to 1V8 _AON
GPIO13	LCD_BLEN	O	Panel Backlight Enable	100K pull-down
GPIO14	HPD_A	I	Hot Plug Detect for IFPA	
GPIO15	HPD_B	I	Hot Plug Detect for IFPB	
GPIO16	SYS_PEX_RST_MON#	O	System side PCIe reset monitor	10K pull-up to 1V8 _AON
GPIO17	HPD_D	I	Hot Plug Detect for IFPD	
GPIO18	HPD_E	I	Hot Plug Detect for IFPE	
GPIO19	3Dvision	O	3D Vision L/R signal	100K pull-down
GPIO20	GC5_MODE			
GPIO21	UNUSED	I/O		
GPIO22	UNUSED	I/O		
GPIO23	GPU_PEX_RST_HOLD#	O	GPU PCIe self-reset control	OD, 10K pull-up to a gated 3V3
GPIO24	HPD_F	I		
GPIO25	UNUSED			
GPIO26	UNUSED			
GPIO27	HPD_C	I	Hot Plug Detect for IFPC	



nVIDIA Power Sequence Control Power on = 1V8\_AON -> 1V8\_MAIN -> 3V3\_NV -> NVVDD -> NVDDS/PEX\_VDD -> FBVDDQ -> DGPUPWRGD

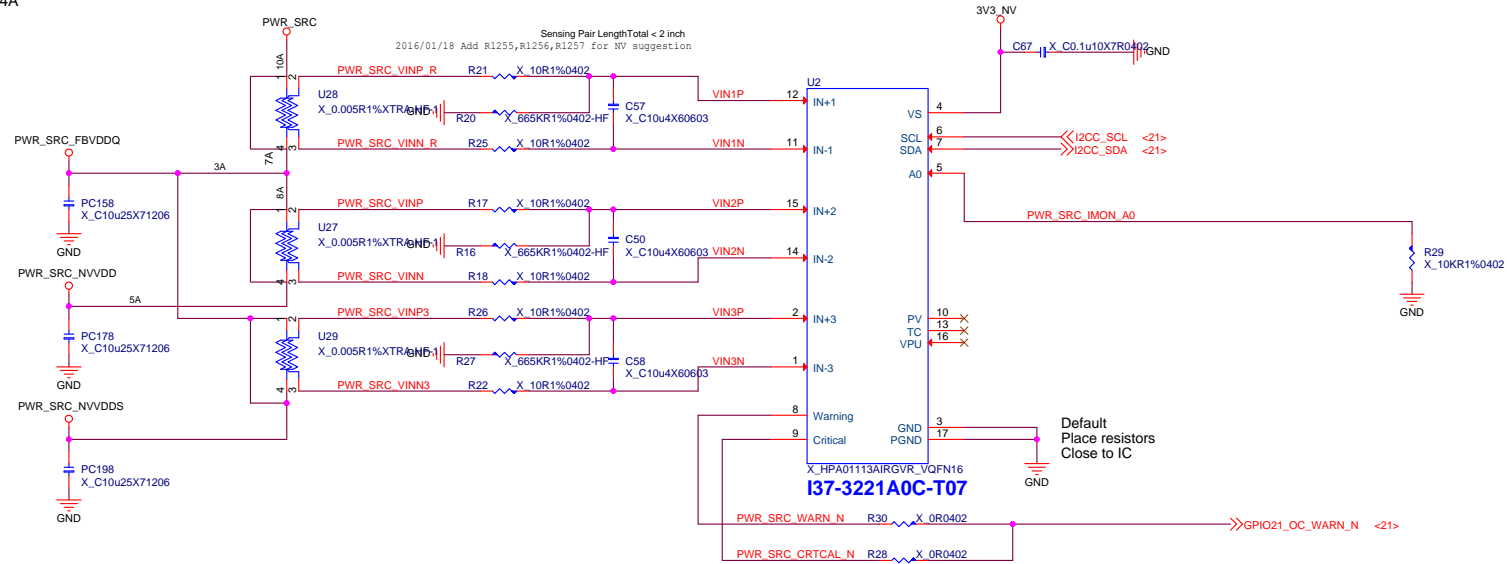


nVIDIA Power Sequence Power Down Power down = FBVDDQ -> NVDDS/PEX\_VDD -> 3V3\_NV -> 1V8\_AON -> 1V8\_MAIN

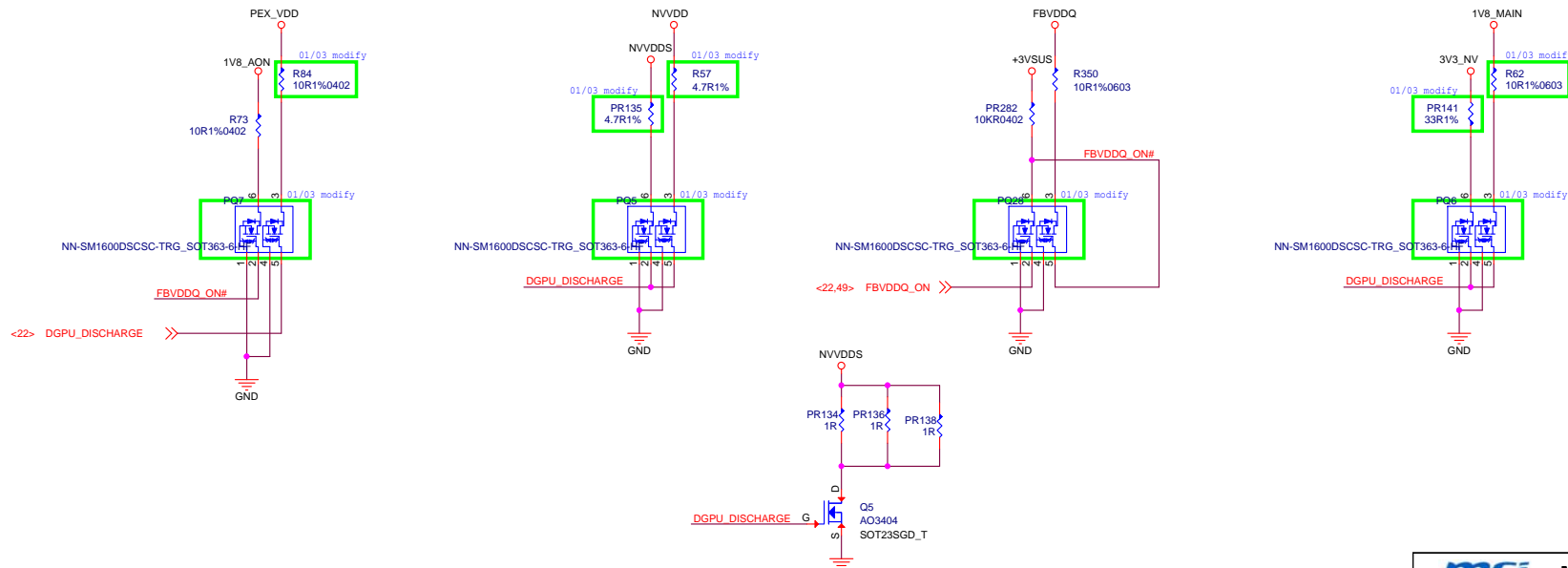


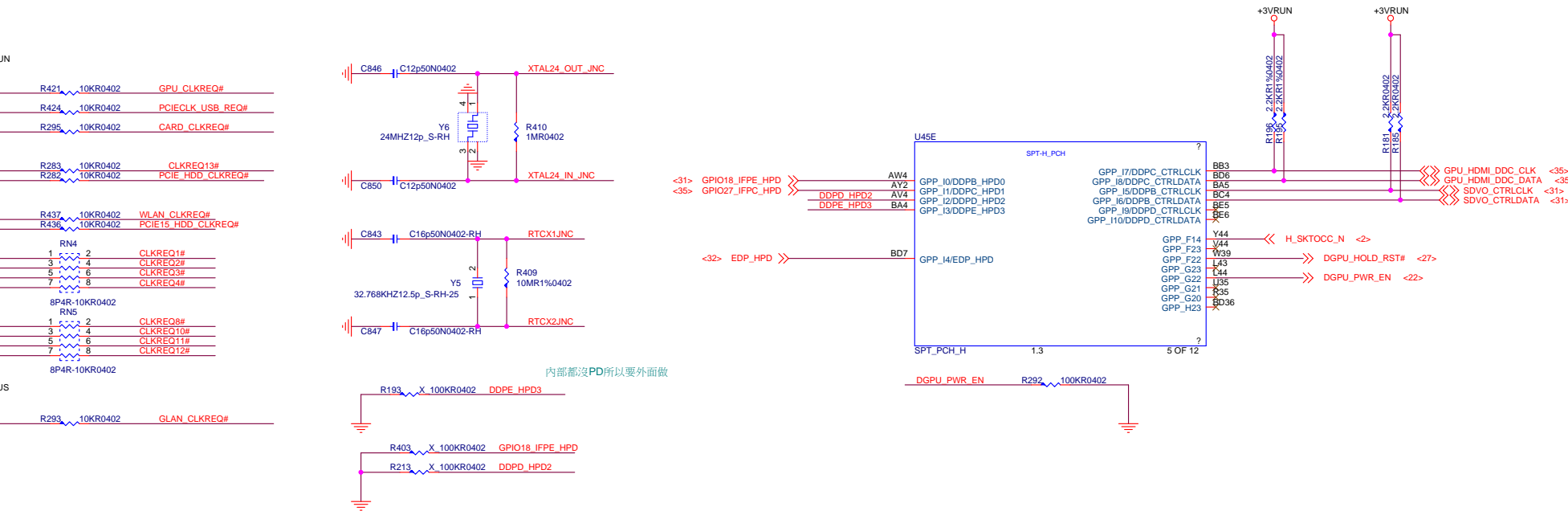
# DGPU\_Power Control

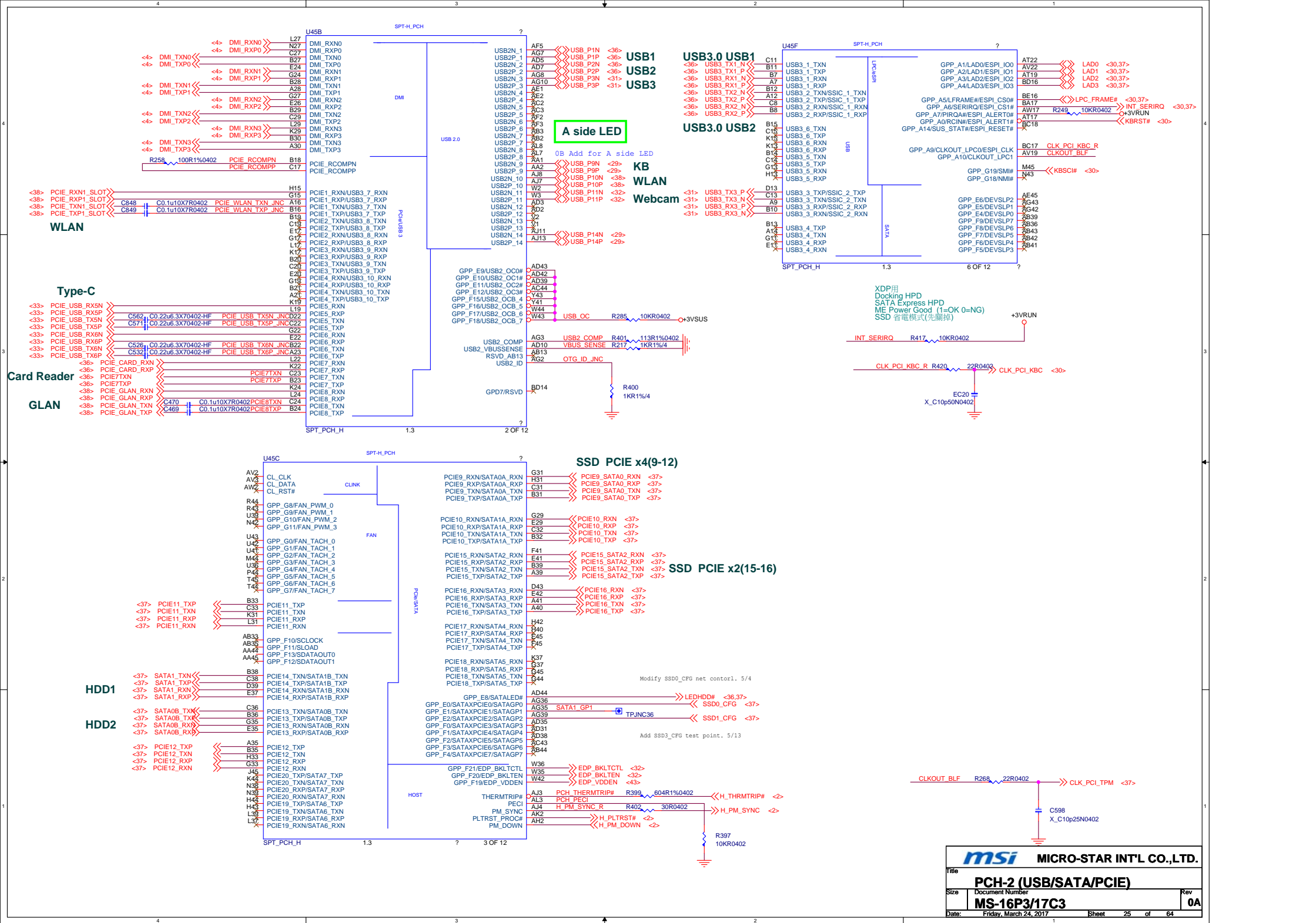
EDP Design Guide:  
N17E-G1(90W)  
NVVDD : 58A ; Peak 136A  
NVVDDS : 28A ; Peak 74A  
1.8V : 0.9A  
PEX\_VDD : 3A  
FBVDDQ : 16A



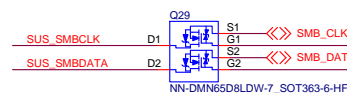
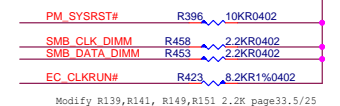
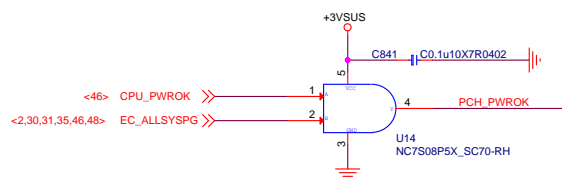
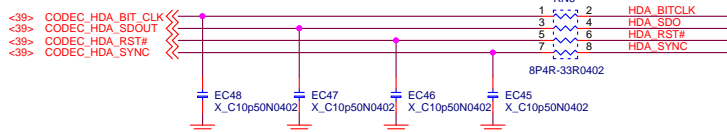
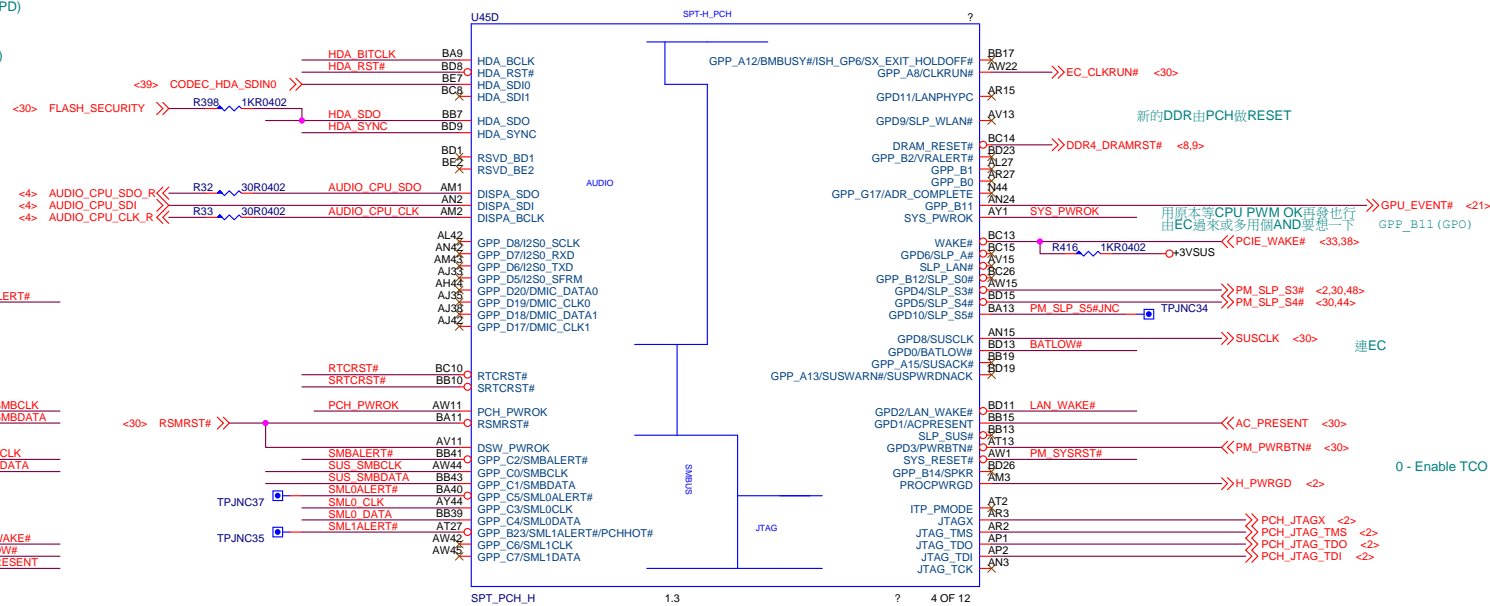
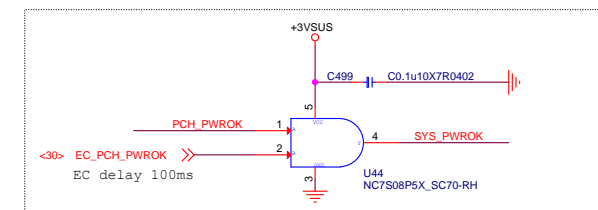
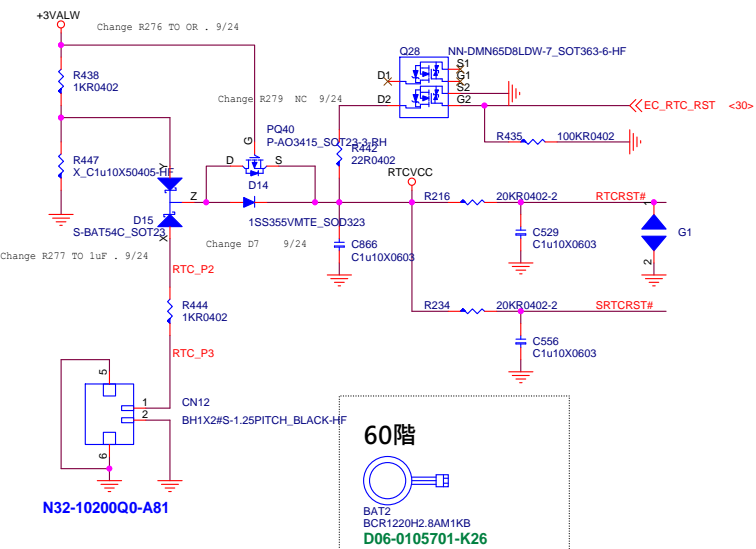
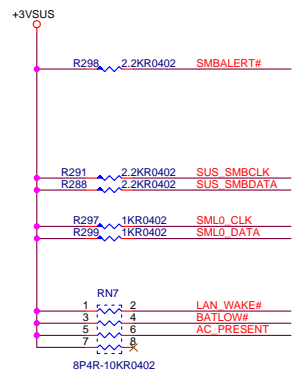
## Discharge







PCH EDS Page 52

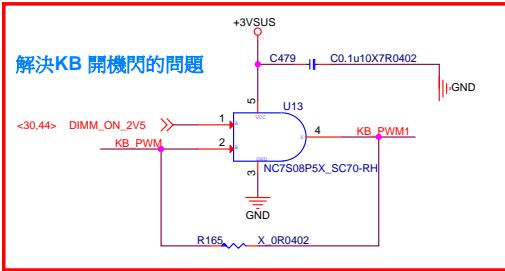
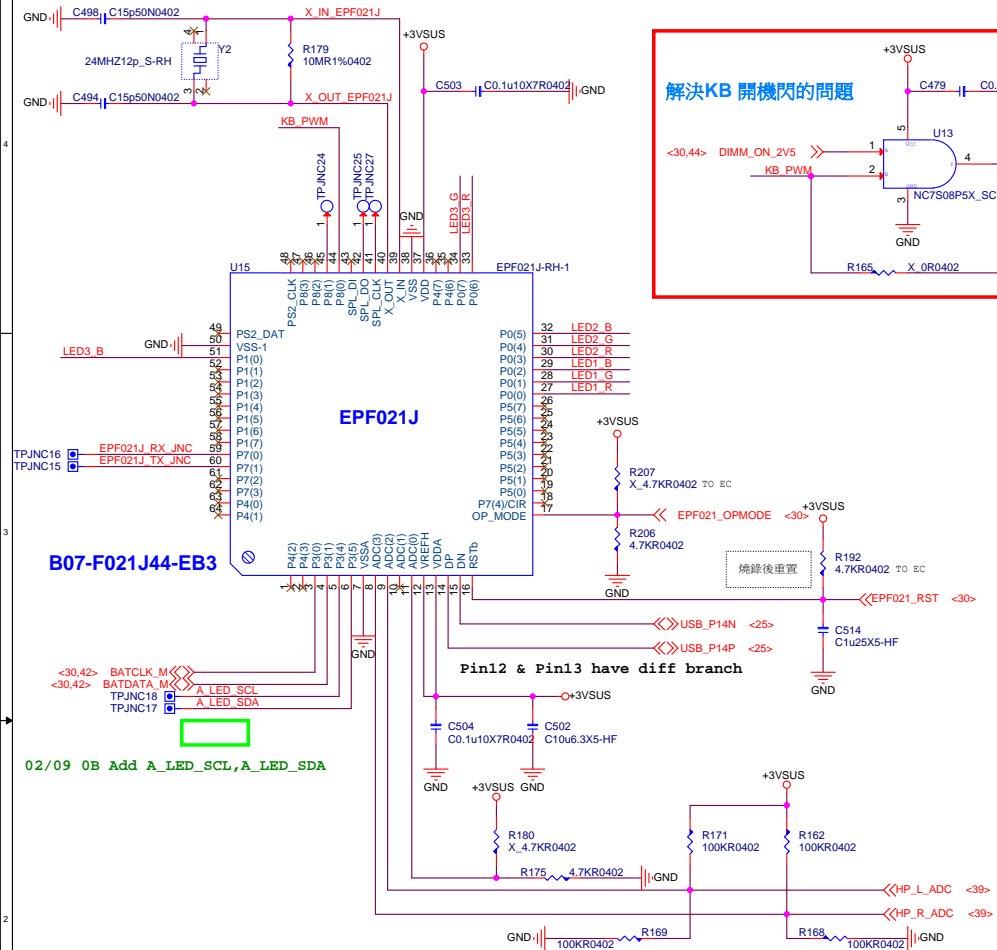




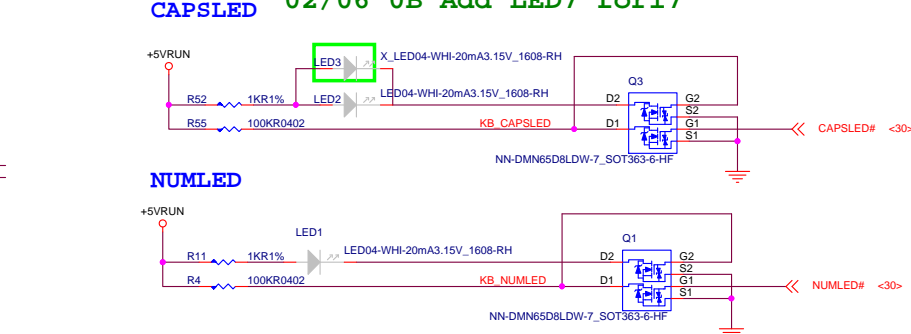
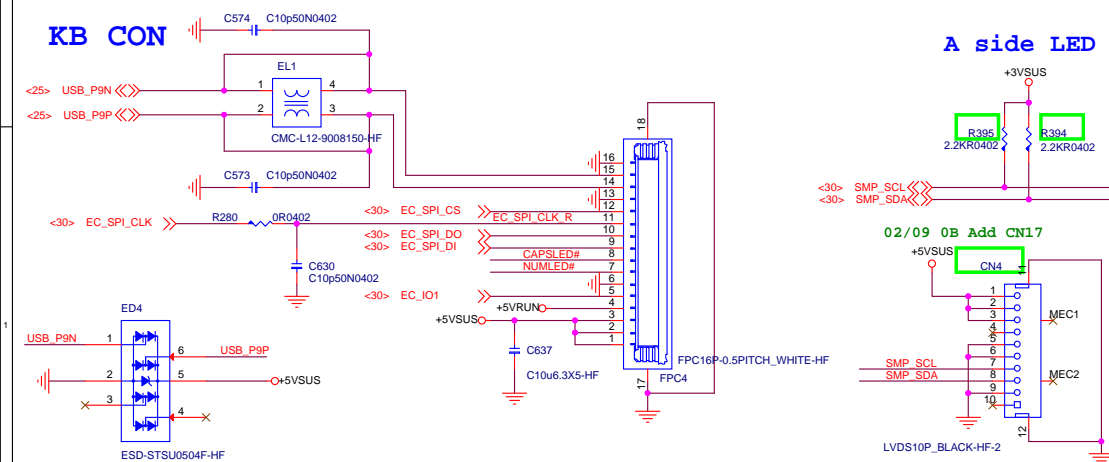
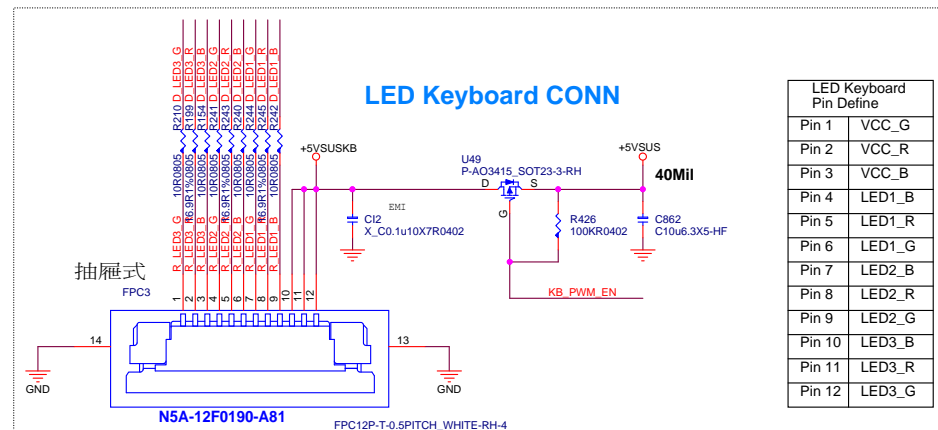
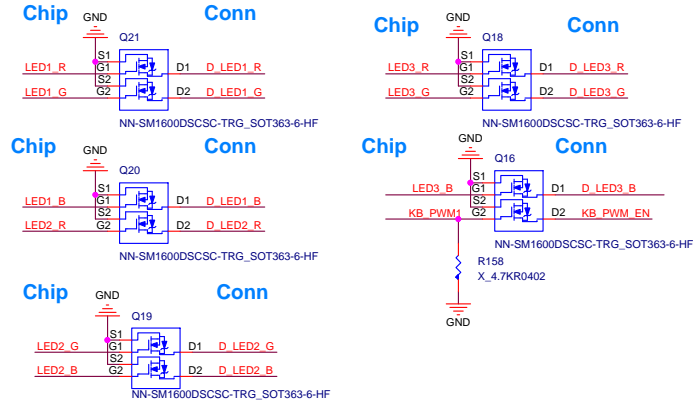




# LED 8051 Controller

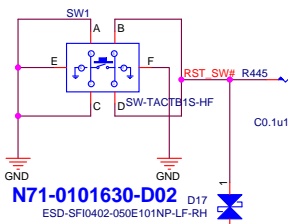


EPF021J Sink current not enough, only using BSS138 (0.22A)

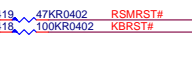


 RSMRST# follow DG modify to 10K

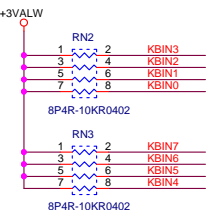
## Hardware Reset



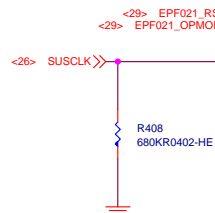
PU/PD



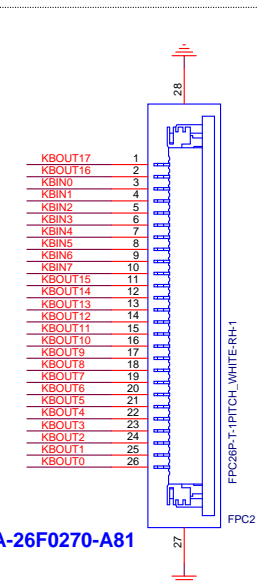
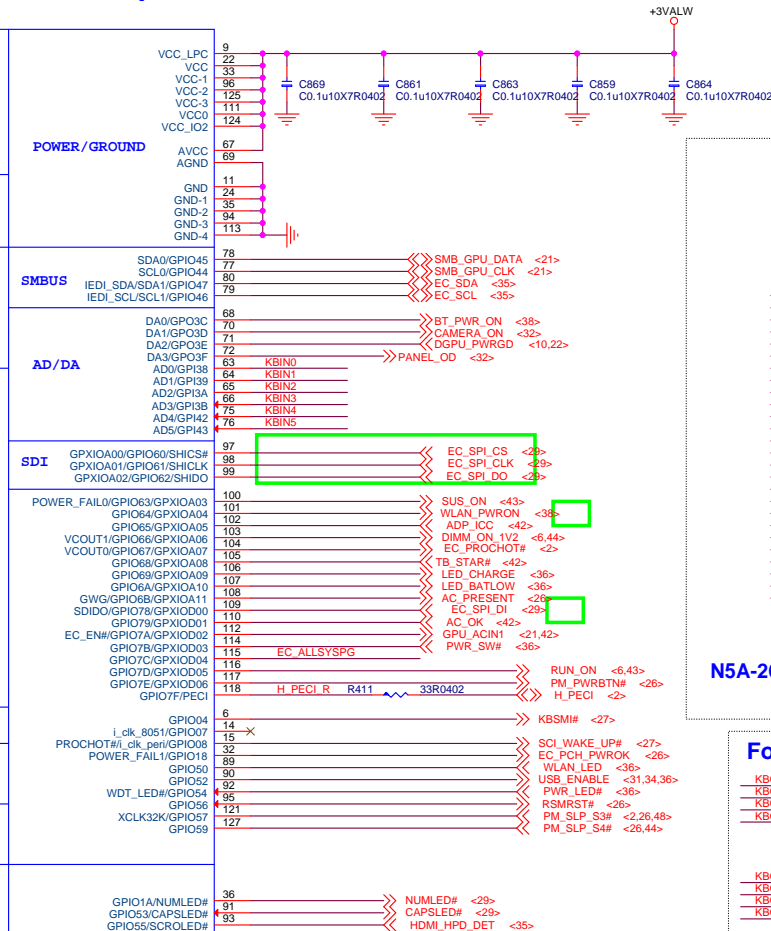
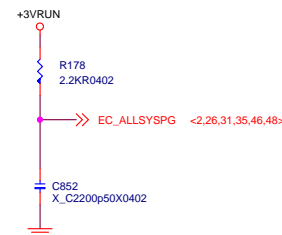
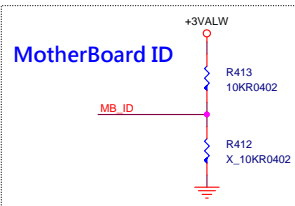
## KB pull Hi 10k



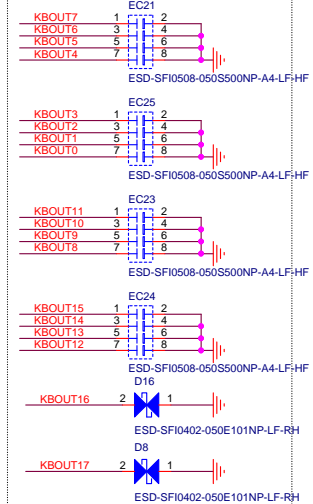
LID pull hi 10K



## MotherBoard ID

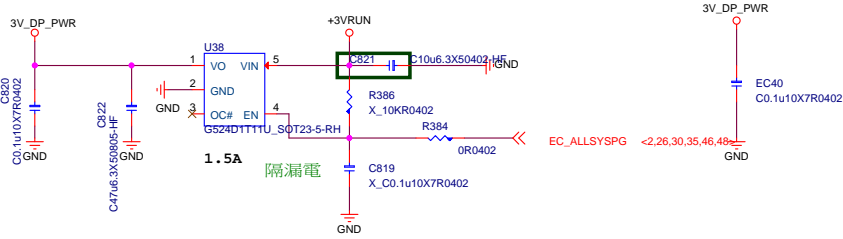


**For EL**

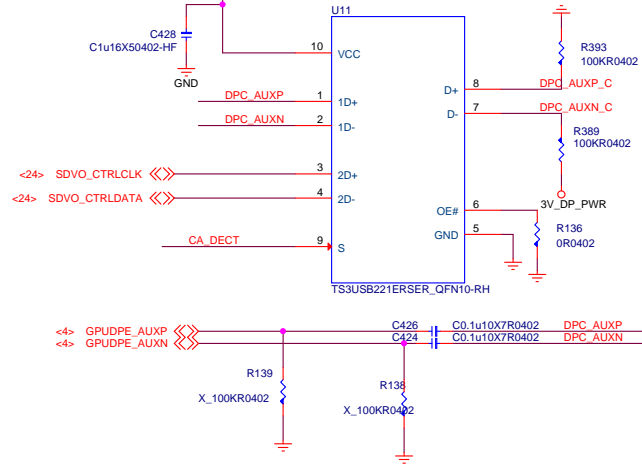


## Display Port

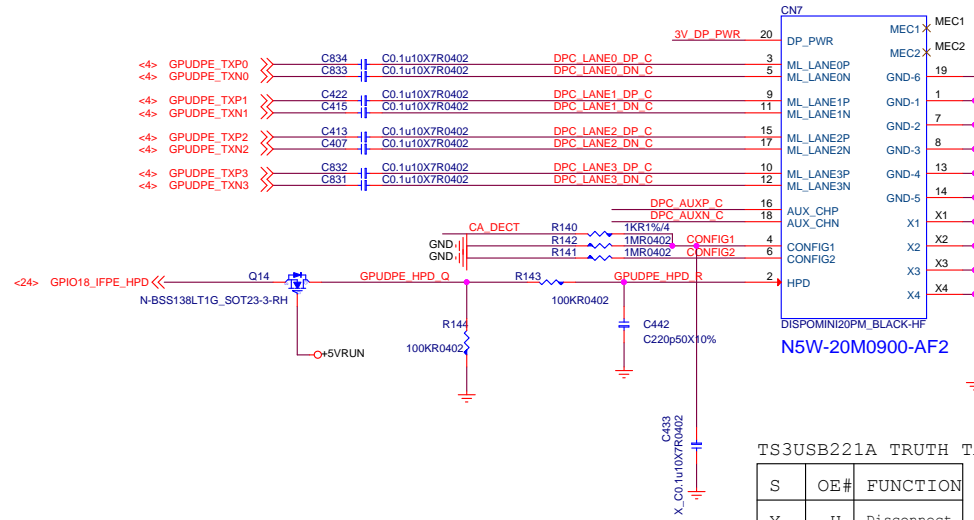
The preset trip limit must not exceed 3A at the Upstream device connector DP\_PWR pin and 1.5A at the Downstream device connector DP\_PWR pin.



## DP/TMDS mode select



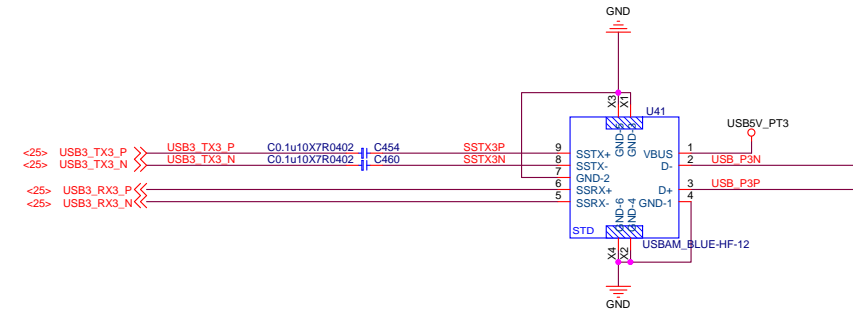
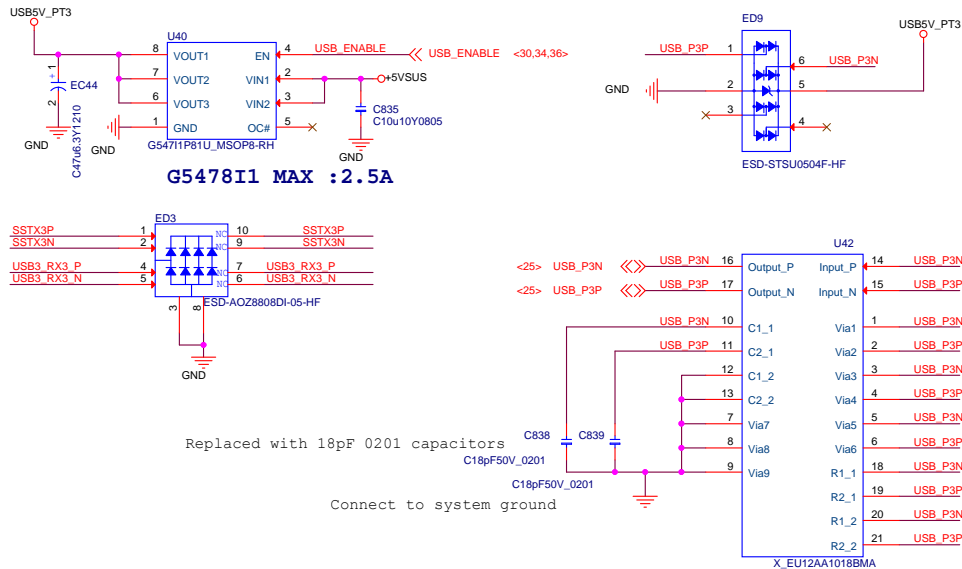
## Display Port



TS3USB221A TRUTH TABLE

S	OE#	FUNCTION
X	H	Disconnect
L	L	D = 1D
H	L	D = 2D

## USB 3.0 CNT 3



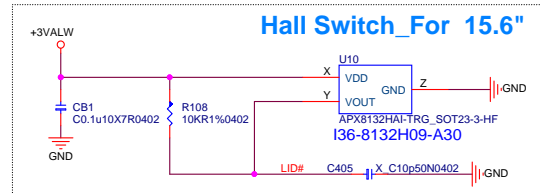
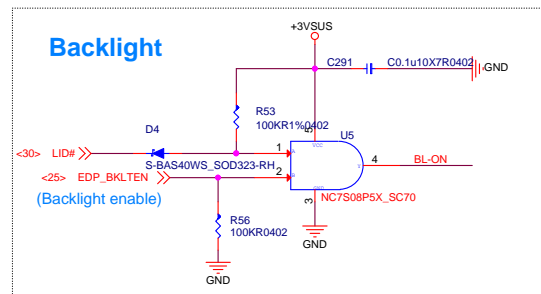
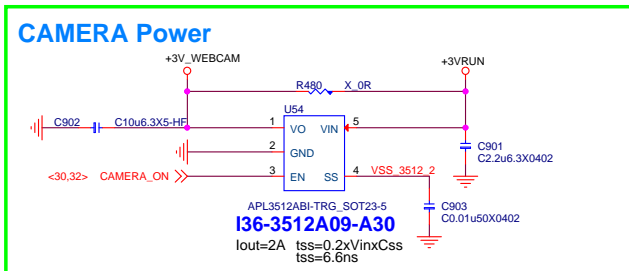
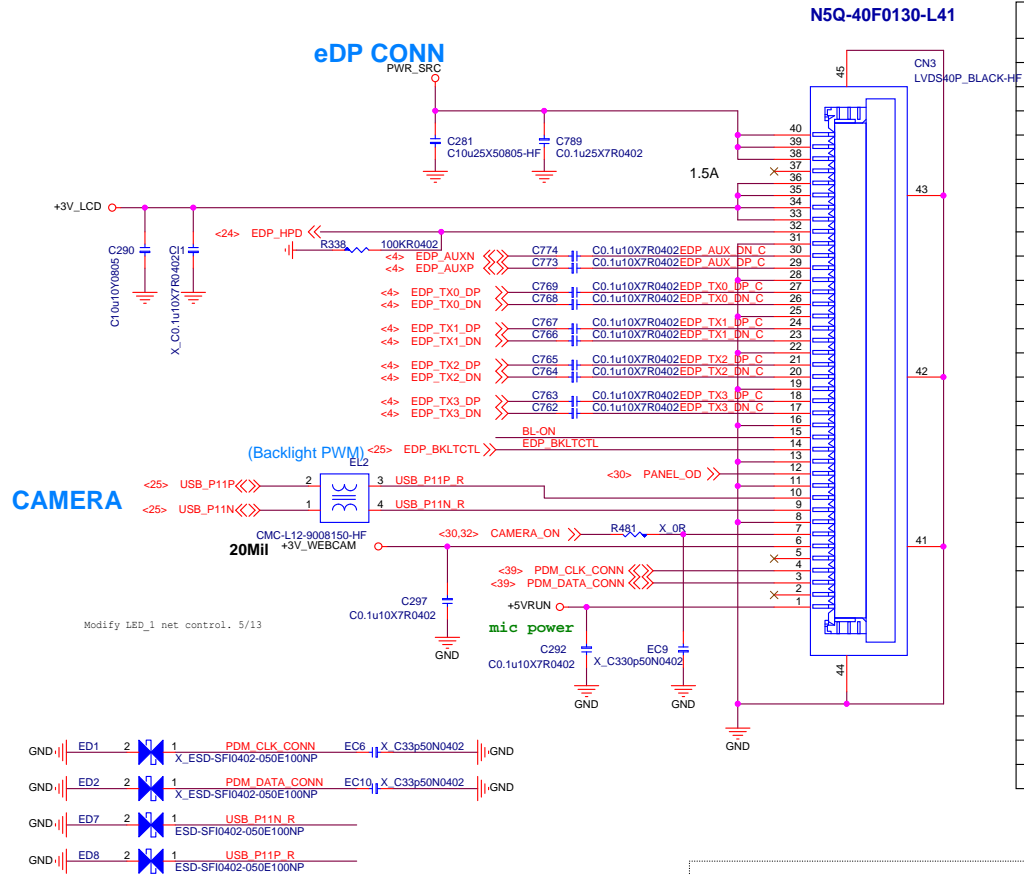
02/02 modify CN12 footprint.

USB3.0	N53-09M0681-AF2
USB3.0_LED	N53-13M0031-L06

## eDP/Camera

## LCD Module Pin Define FOR FULL HD PANEL

### LCD Module Pin Define FOR WQHD PANEL

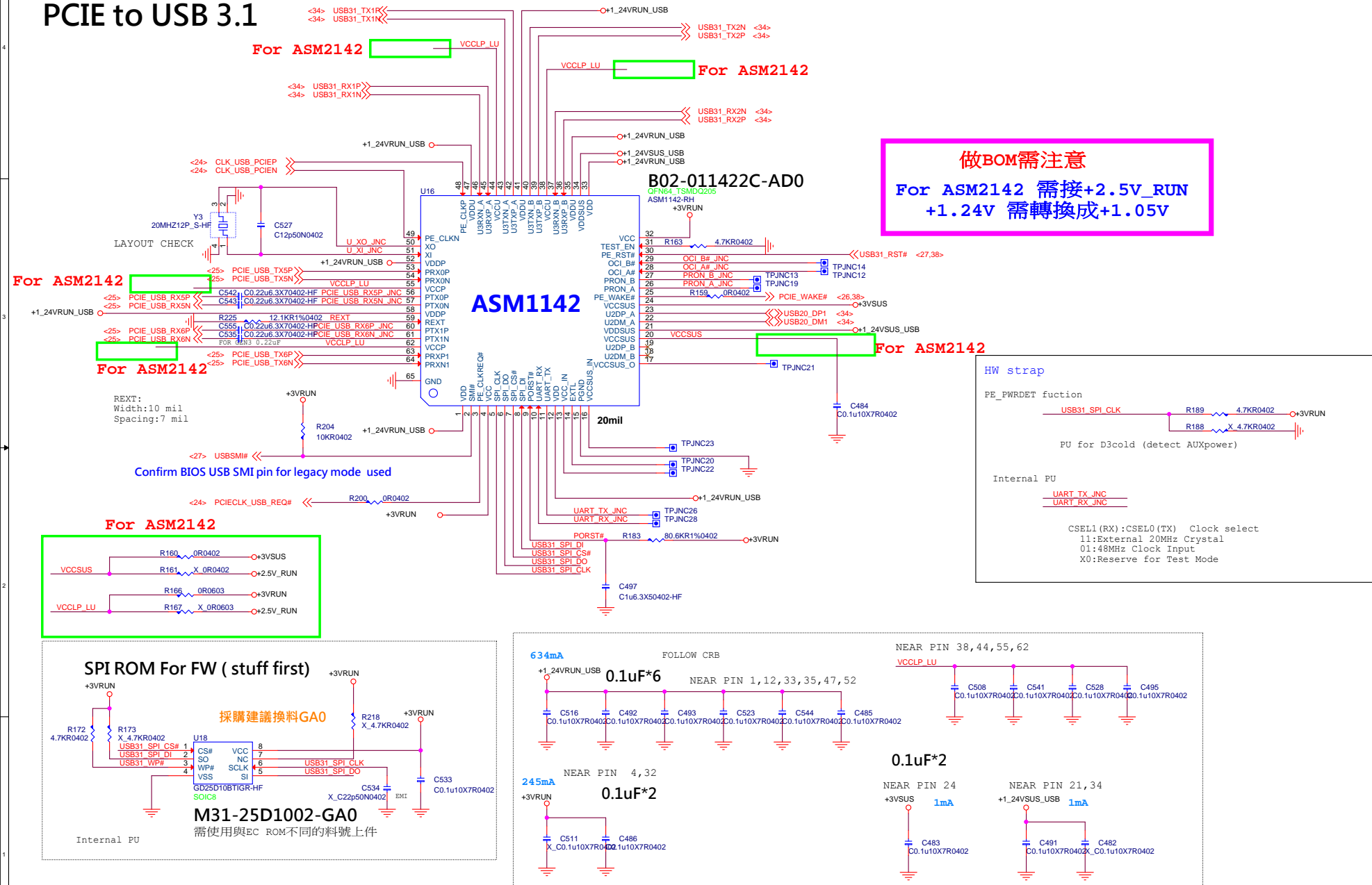


Pin No	Symbol	Description
1	Vcom SDA	Vcom IIC SDA
2	H_GND	High Speed Ground
3	LAN1_N	Complement Signal-Lane 1
4	LAN1_P	True Signal-Main Lane 1
5	H_GND	High Speed Ground
6	LAN0_N	Complement Signal-Lane 0
7	LAN0_P	True Signal-Main Lane 0
8	H_GND	High Speed Ground
9	AUX+	True Signal-Auxiliary Channel
10	AUX-	Complement Signal-Auxiliary Channel
11	H_GND	High Speed Ground
12	LCD_VCC	Power Supply +3.3 V (typical)
13	LCD_VCC	Power Supply +3.3 V (typical)
14	NC	No Connection (Reserved for CMI test)
15	H_GND	Ground
16	H_GND	Ground
17	HPD	Hot Plug Detect
18	BL_GND	BL Ground
19	BL_GND	BL Ground
20	BL_GND	BL Ground
21	BL_GND	BL Ground
22	BL_EN	BL_Enable Signal of LED Converter
23	BL_PWM	PWM Dimming Control Signal of LED Converter
24	Vcom SCL	Vcom IIC SCL
25	NC	No Connection (Reserved)
26	LED_VCCS	BL Power
27	LED_VCCS	BL Power
28	LED_VCCS	BL Power
29	LED_VCCS	BL Power
30	OE_EN	OD_Enable Signal of TCON

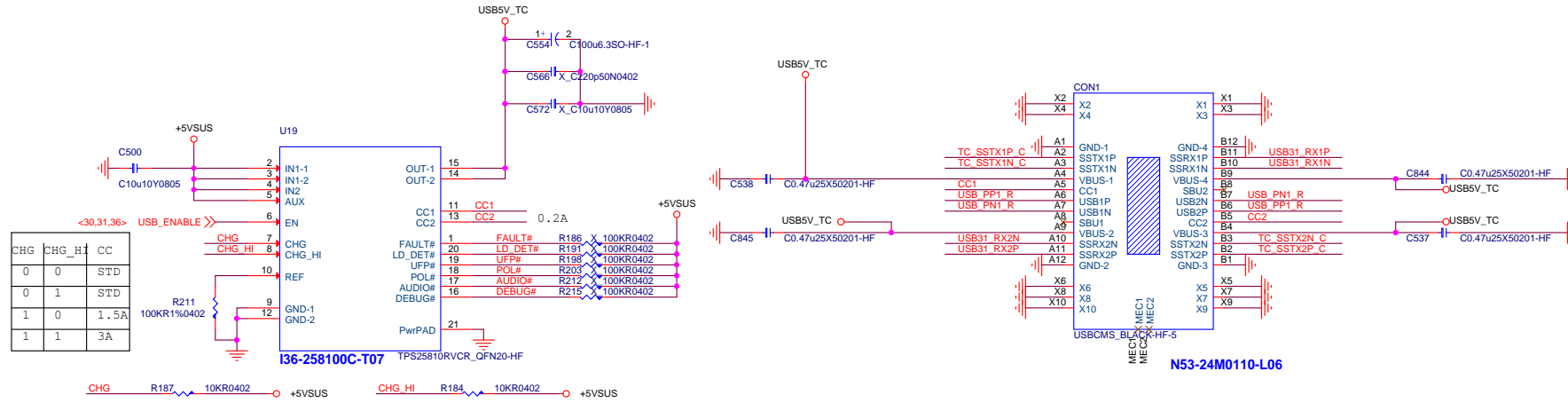
Pin No	Symbol	Description
1	NC	Reserved for LCD manufactureer's use
2	H_GND	High Speed Ground
3	Lane3_N	Complement Signal Link Lane 3
4	Lane3_P	True Signal Link Lane 3
5	H_GND	High Speed Ground
6	Lane2_N	Complement Signal Link Lane 2
7	Lane2_P	True Signal Link Lane 2
8	H_GND	High Speed Ground
9	Lane1_N	Complement Signal Link Lane 1
10	Lane1_P	True Signal Link Lane 1
11	H_GND	High Speed Ground
12	Lane0_N	Complement Signal Link Lane 0
13	Lane0_P	True Signal Link Lane 0
14	H_GND	High Speed Ground
15	AUX_CH_P	True Signal Auxiliary Channel
16	AUX_CH_N	Complement Signal Auxiliary Channel
17	H_GND	High Speed Ground
18	VDD	LCD logic and driver power(3.3V)
19	VDD	LCD logic and driver power(3.3V)
20	VDD	LCD logic and driver power(3.3V)
21	VDD	LCD logic and driver power(3.3V)
22	BIST	BIST patterns selection L : Disable [default] , H : Enable
23	LCD_GND	LCD logic and driver ground
24	LCD_GND	LCD logic and driver ground
25	LCD_GND	LCD logic and driver ground
26	LCD_GND	LCD logic and driver ground
27	HPD	HPD signal pin
28	BL_GND	Backlight ground
29	BL_GND	Backlight ground
30	BL_GND	Backlight ground
31	BL_GND	Backlight ground
32	BL_ENABLE	Backlight On/Off
33	BL_PWM_DIM	System PWM
34	NC	Reserved for LCD manufacturer's use
35	NC	Reserved for LCD manufacturer's use
36	VBL	Backlight power
37	VBL	Backlight power
38	VBL	Backlight power
39	VBL	Backlight power
40	OE_EN	OD_Enable Signal of TCON



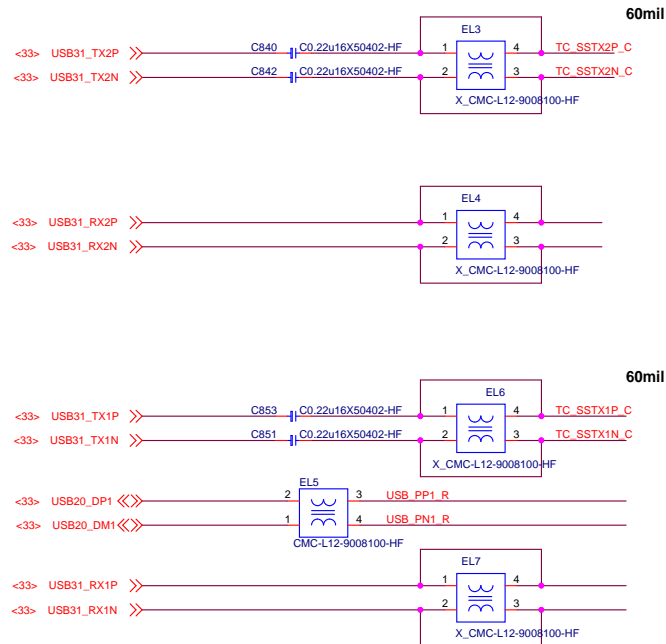
## PCIE to USB 3.1



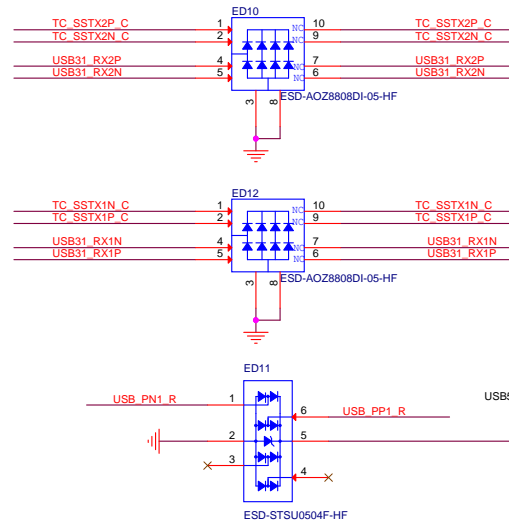
# Type C



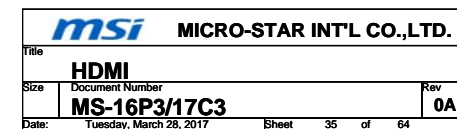
## USB3.1 TYPE C



for EMI

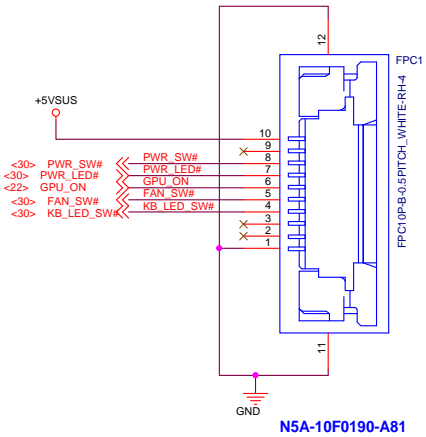


## HPD\_SNK Internal PD 150kohm

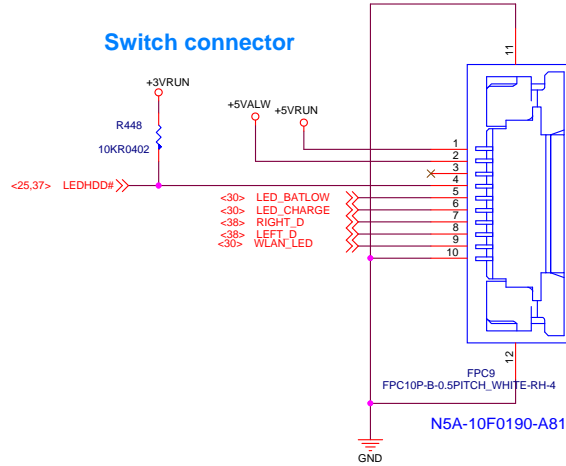


# CPU FAN/CPU FAN/POWER CONN/ LED CONN

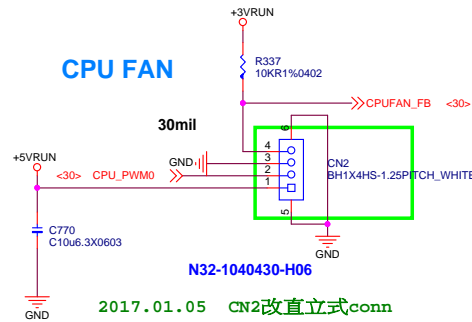
## Power Switch Connector



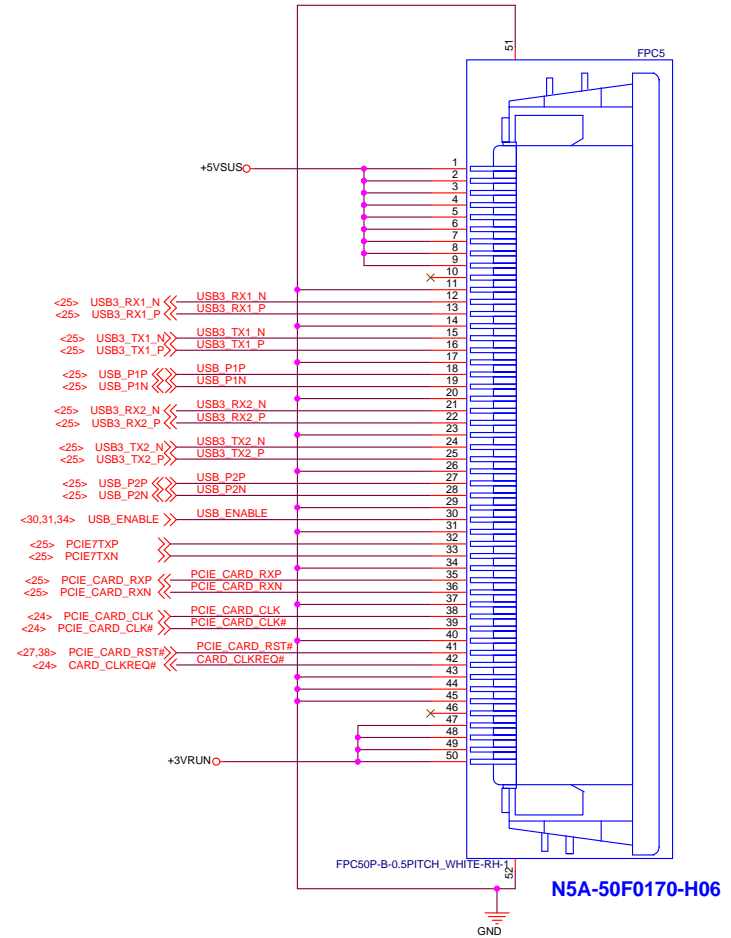
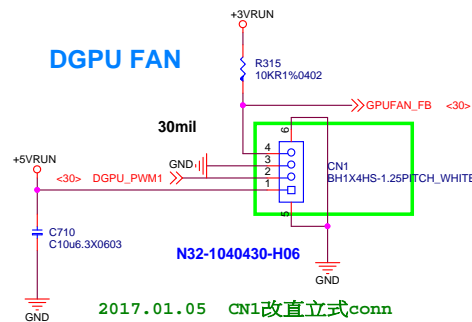
## Switch connector



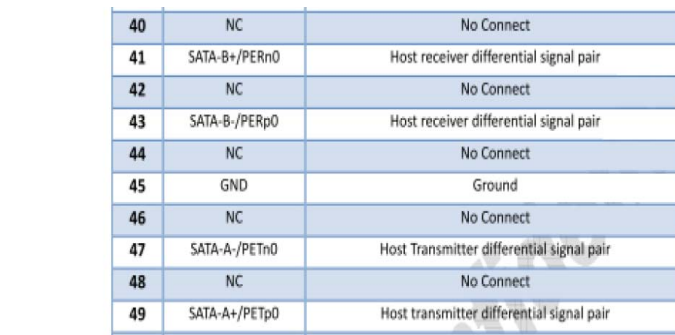
## CPU FAN



## DGPU FAN



PCIEx4 /SATA SSD



PCIEx2 /SATA SSD

The diagram illustrates the pin connections for the N15-0670320-CK3 connector. It shows a central connector block with pins numbered 1 through 75. Various components are connected to these pins, including LEDs (LEDHDD#, LEDSSD), SSDs (SSD1\_DEVSLP, SSD1\_RST#, SSD1\_OFG), SATA drives (SATA0\_RXP, SATA0\_RXN, SATA0\_TXN, SATA0\_TXP), and power/ground connections (+3VRUN, GND). Specific components like C586, C587, C588, C882, C871, C881, C870, R289, R281, EC28, C634, and C633 are labeled. The diagram also shows the connection of the connector to the N15-0670320-CK3 board.

SCREW1  
E43-1205022-H29

SCREW2  
E43-1205022-H29

+5VRUN

200mil (5A)

C167  
C22u6.3X0.003

C179  
X\_C220p50ND402

SATA1\_TXP  
C187  
C0.01u16X0402

SATA1\_TXN  
C186  
C0.01u16X0402

SATA1\_RXN  
C189  
C0.01u16X0402

SATA1\_RXP  
C188  
C0.01u16X0402

SATA1\_TXP\_JNC  
SATA1\_TXN\_JNC  
SATA1\_RXN\_JNC  
SATA1\_RXP\_JNC

MEC  
MEC

SATA0B\_TXP  
SATA0B\_TXN  
SATA0B\_RXN  
SATA0B\_RXP

FPC7  
11

N5N-22F0401-AF2

N5A-10F0190-A81

(Must used the gold fresh type)

<25,30> LAD0 <<>> 26 LAD0

<25,30> LAD1 <<>> 27 LAD1

<25,30> LAD2 <<>> 28 LAD2

<25,30> LAD3 <<>> 29 LAD3

<25,30> LPC\_FRAME# <<>> 22 LFRAME#

<27,30> TPM\_RST# <<>> 16 LRESET#

<25,30> INT\_SERIRQ <<>> 15 NC-9

<25> CLK\_PCI\_TPM <<>> 27 SERIRQ

<25> <<>> 21 LCLK

+3VRUN

R261 10KR0402

PP

R265 10KR0402

U20

GPIO 6

VDD-3 18

VDD-4 25

VDD-2 10

VDD-1 5

GND-3 18

GND-4 11

GND-2 4

NC-8 14

NC-7 13

NC-6 12

NC-3 10

NC-1 3

SLB9665TT2.0-RH-1

+3VRUN

C575 C0.1u10X7R0402

C579 C0.1u10X7R0402

C585 C0.1u10X7R0402

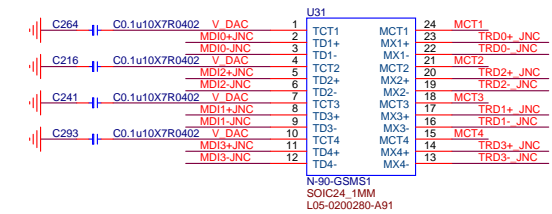
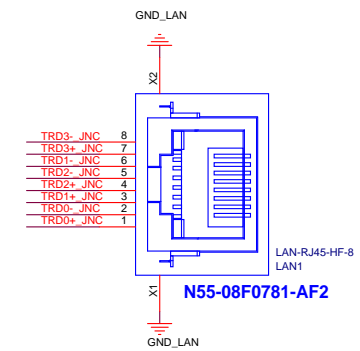
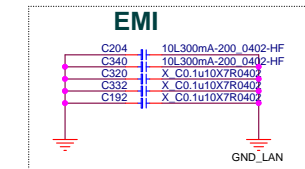
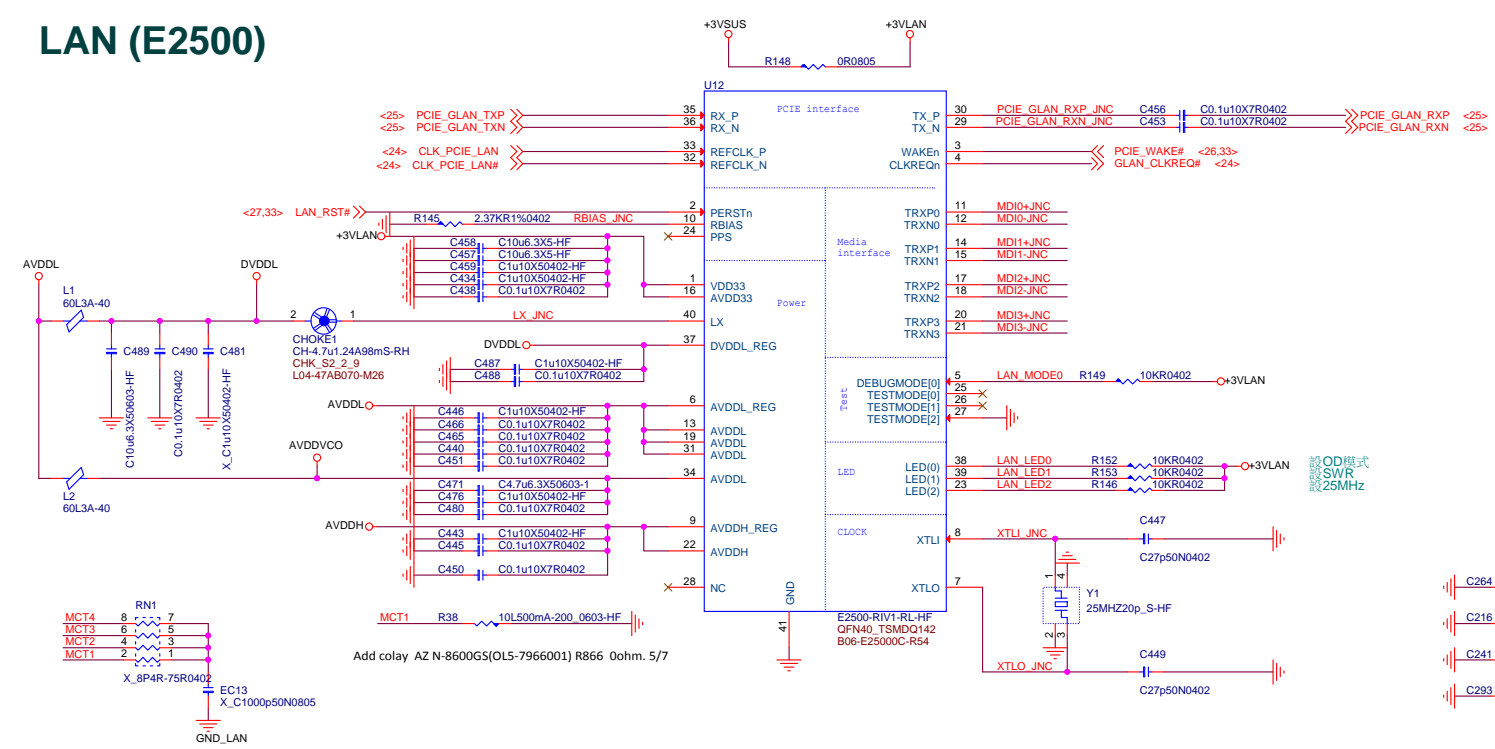
C599 C0.1u10X7R0402

File

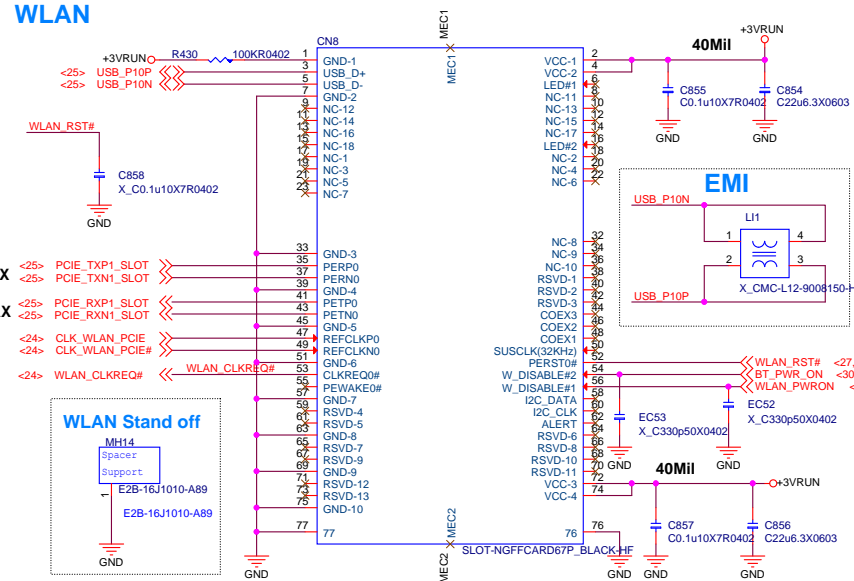
**msi** MICRO-STAR INT'L CO.,L

**M2 SSD/HDD/TPM**

# LAN (E2500)

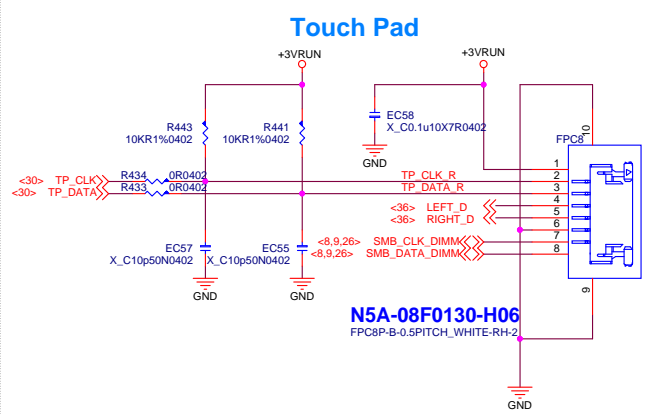


# WLAN



# WLAN /Touch Pad

Pin 1	GND	Pin 2	3.3V
Pin 3	USB_D+	Pin 4	3.3V
Pin 5	USB_D-	Pin 6	LED1#
Pin 7	GND	Pin 8	Module Key
Pin 9	Module Key	Pin 10	Module Key
Pin 11	Module Key	Pin 12	Module Key
Pin 13	Module Key	Pin 14	Module Key
Pin 15	Module Key	Pin 16	Module Key
Pin 17	N/C	Pin 18	GND
Pin 19	N/C	Pin 20	N/C
Pin 21	N/C	Pin 22	N/C
Pin 23	N/C	Pin 24	Module Key
Pin 25	Module Key	Pin 26	Module Key
Pin 27	Module Key	Pin 28	Module Key
Pin 29	Module Key	Pin 30	Module Key
Pin 31	Module Key	Pin 32	N/C
Pin 33	GND	Pin 34	N/C
Pin 35	PERP0	Pin 36	N/C
Pin 37	PERN0	Pin 38	Clink Reset (I 3.3V)
Pin 39	GND	Pin 40	N/C
Pin 41	PETP0	Pin 42	N/C
Pin 43	PETN0	Pin 44	N/C
Pin 45	GND	Pin 46	N/C
Pin 47	REFCLKP0	Pin 48	N/C
Pin 49	REFCLKN0	Pin 50	N/C (SUSCLK (32kHz) for DSx)
Pin 51	GND	Pin 52	PERST0#
Pin 53	CLKREQ0#	Pin 54	BT_EN (W_DISABLE2#)
Pin 55	PEWAKE0#	Pin 56	WLAN_EN (W_DISABLE2#)
Pin 57	GND	Pin 58	N/C
Pin 59	N/C	Pin 60	N/C
Pin 61	N/C	Pin 62	N/C
Pin 63	GND	Pin 64	Resever
Pin 65	N/C	Pin 66	N/C
Pin 67	N/C	Pin 68	N/C
Pin 69	N/C	Pin 70	N/C
Pin 71	N/C	Pin 72	3.3V
Pin 73	N/C	Pin 74	3.3V
Pin 75	GND		



N15-0670260-L06  
SLOT\_NGFFCARD67\_15





02/13 0b C795,C777 change to C11-1062617-S02

02/17 R165 NC,R170 上件

0b modify I2C\_SDA,I2C\_SCL

02/17 R242,R236,R235 change to 0R

03/21 1.0 modify MUTE#\_SPK

PDBJD  
Active low to shutdown AMP (L= shutdown ; H= normal)

### Internal Speaker Conn

### Internal woofer Conn

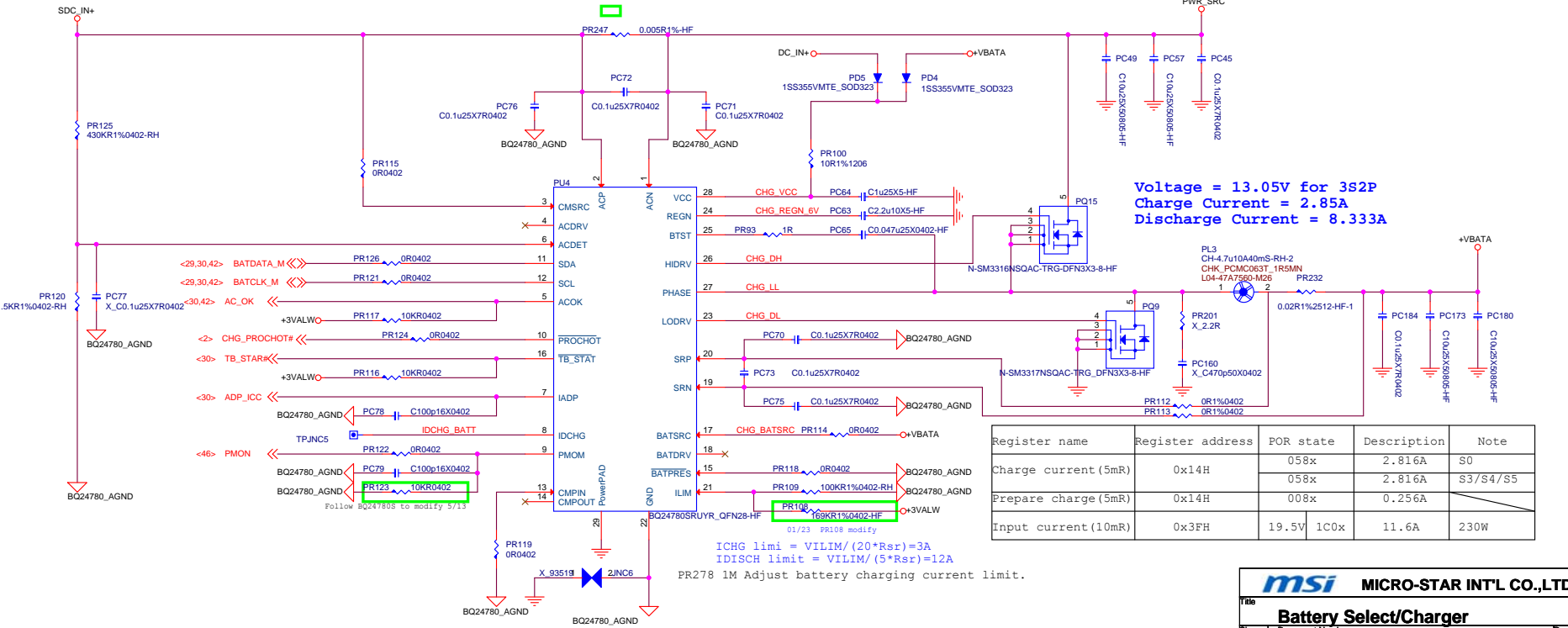
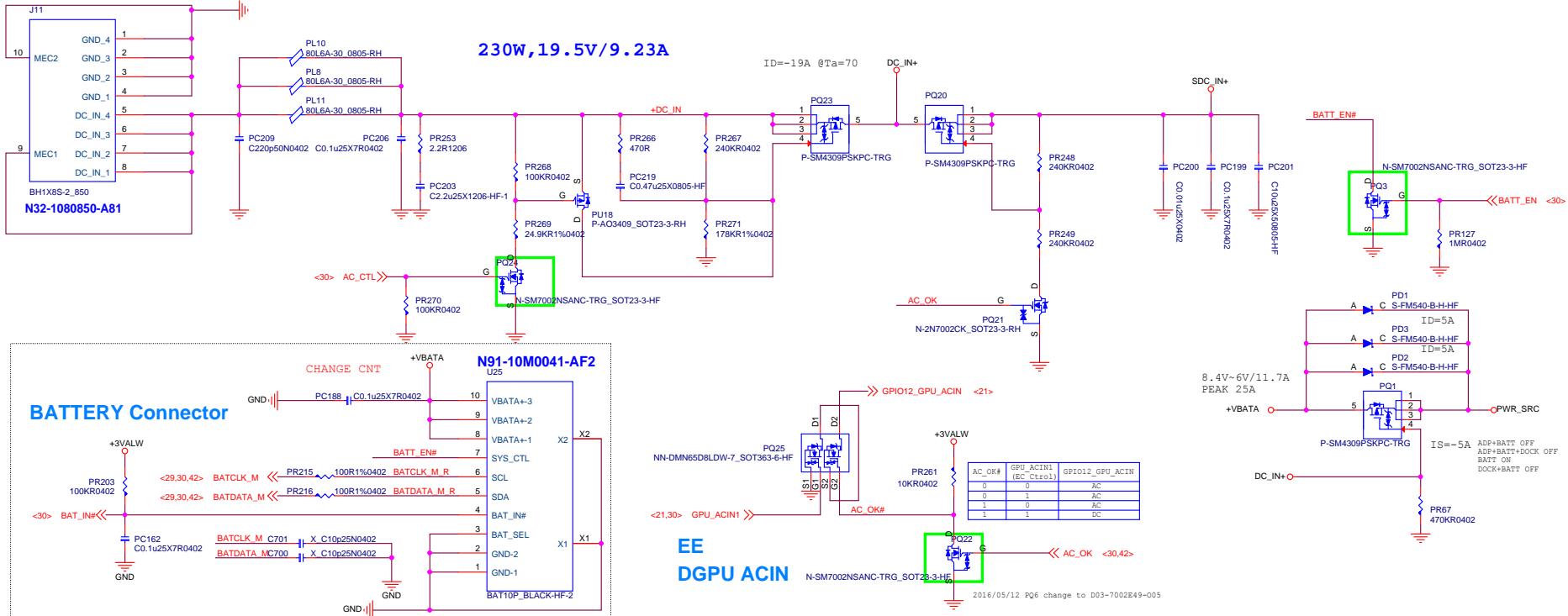
N32-1080280-A81

I2C address selection (L= 0x20H ; H= 0x22H)

U22  
ALC1306

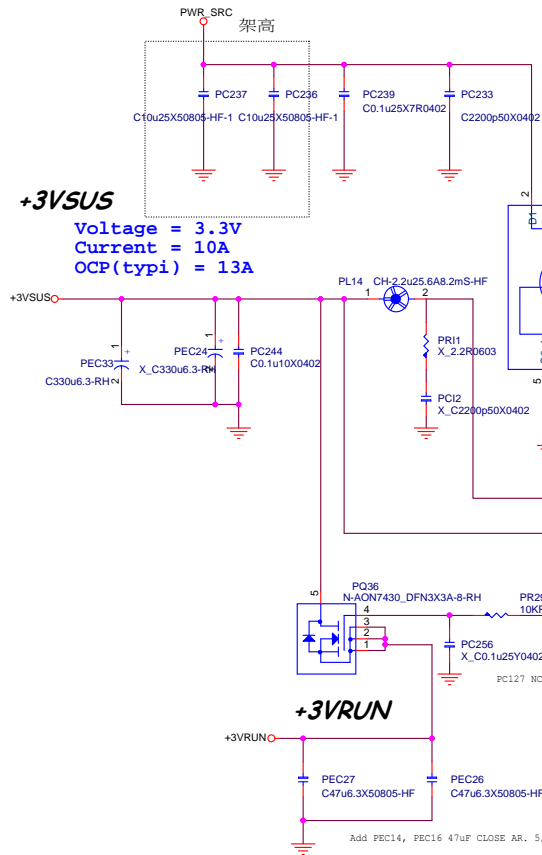
msi MICRO-STAR INT'L CO.,LTD.	
Title	
Speaker	
Size	Document Number
MS-16P3/17C3	
Date:	Rev
Tuesday, March 28, 2017	0A
Sheet	40 of 64



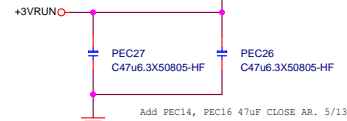


## +3VSUS

Voltage = 3.3V  
Current = 10A  
OCP(typi) = 13A



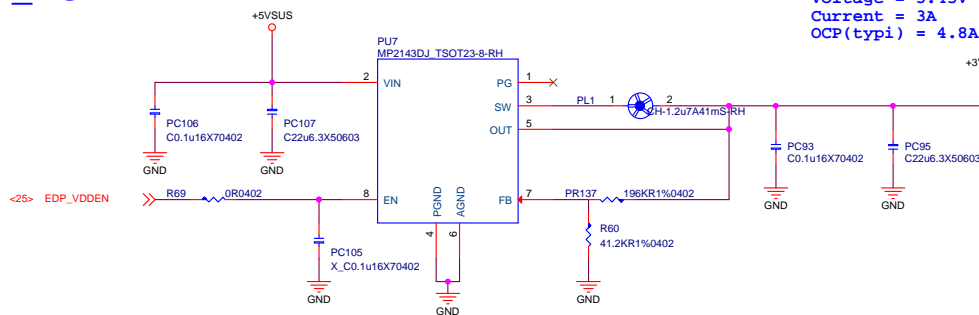
## +3VRUN



## +3V\_LCD

### Panel Device Logic Power

Voltage = 3.45V  
Current = 3A  
OCP(typi) = 4.8A

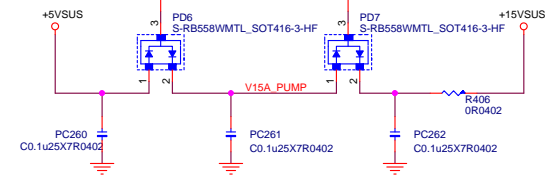


## +3VALW

## +5VALW

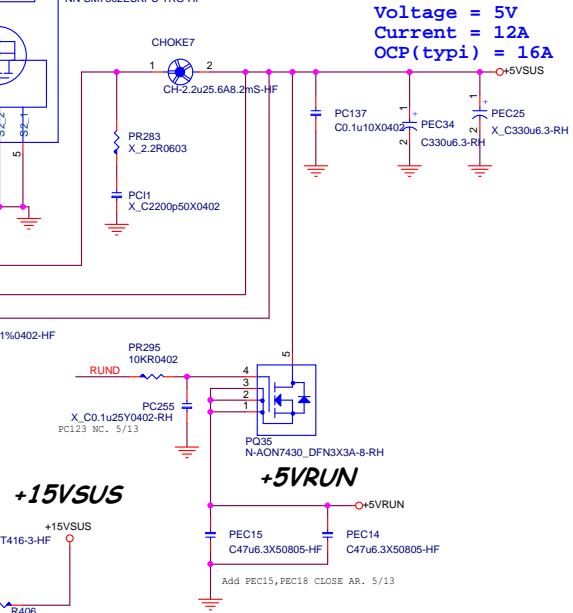


## +15VSUS

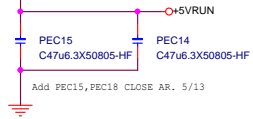


## +5.1VSUS

Voltage = 5V  
Current = 12A  
OCP(typi) = 16A



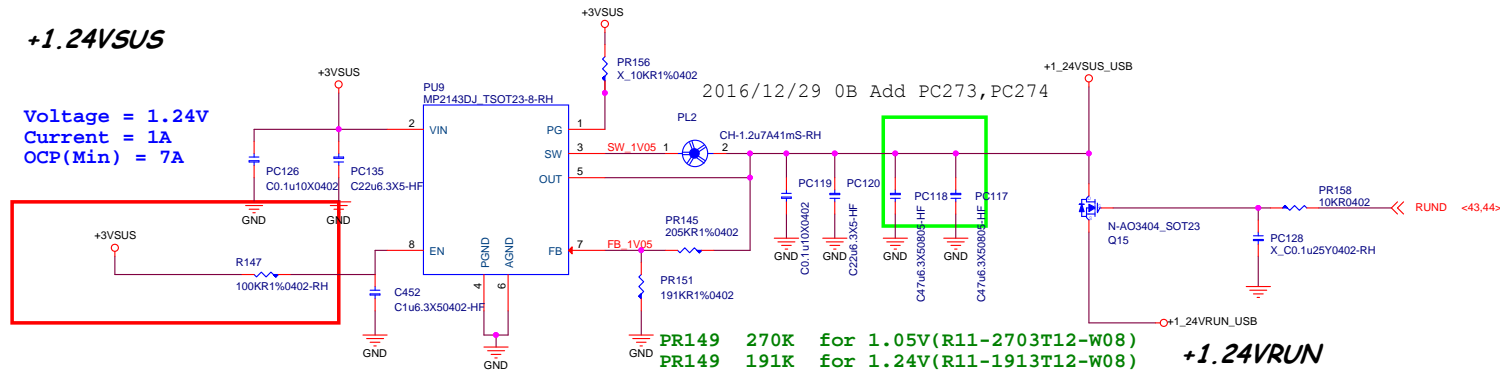
## +5VRUN



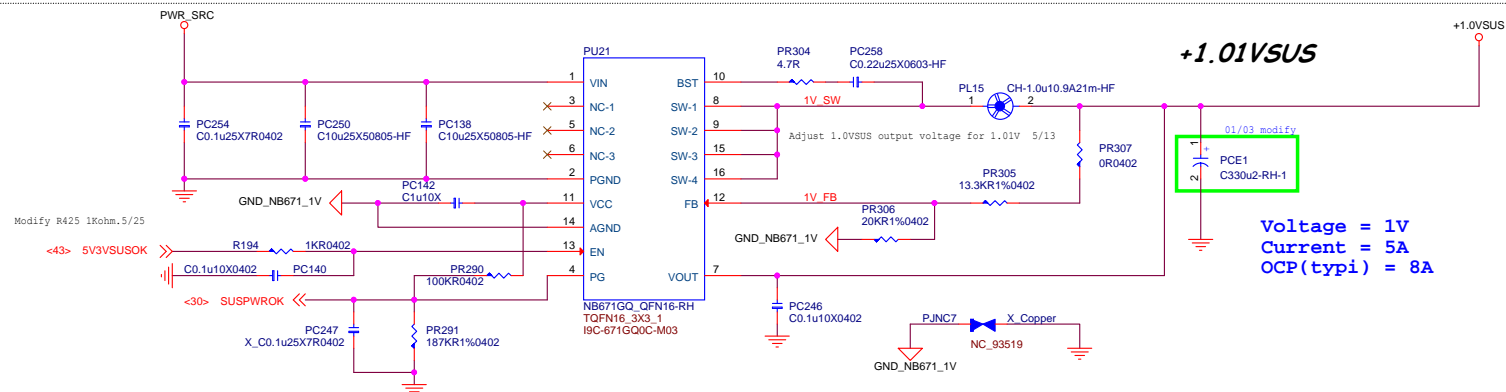


## +1.24VSUS

Voltage = 1.24V  
Current = 1A  
OCP(Min) = 7A

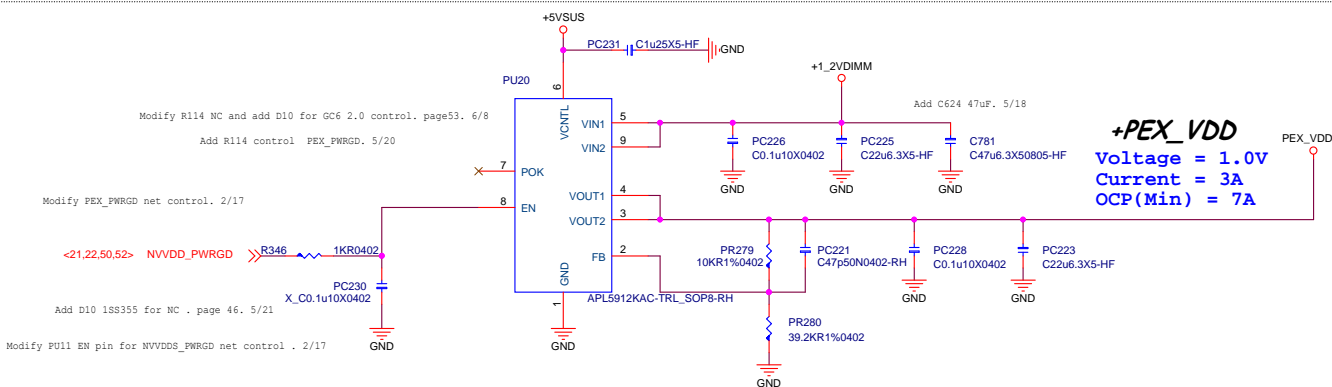


## +1.24VRUN



Voltage = 1V  
Current = 5A  
OCP(typi) = 8A

## +1.01VSUS

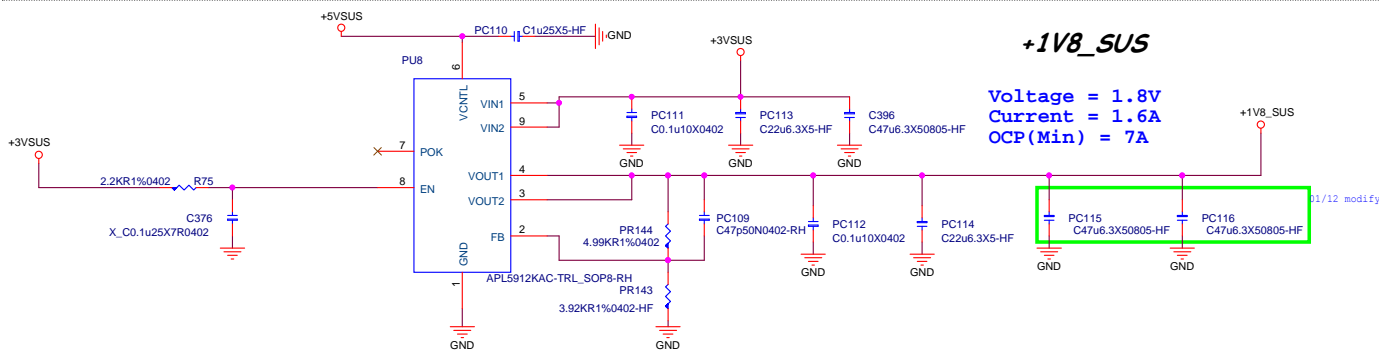


## +PEX\_VDD

Voltage = 1.0V  
Current = 3A  
OCP(Min) = 7A

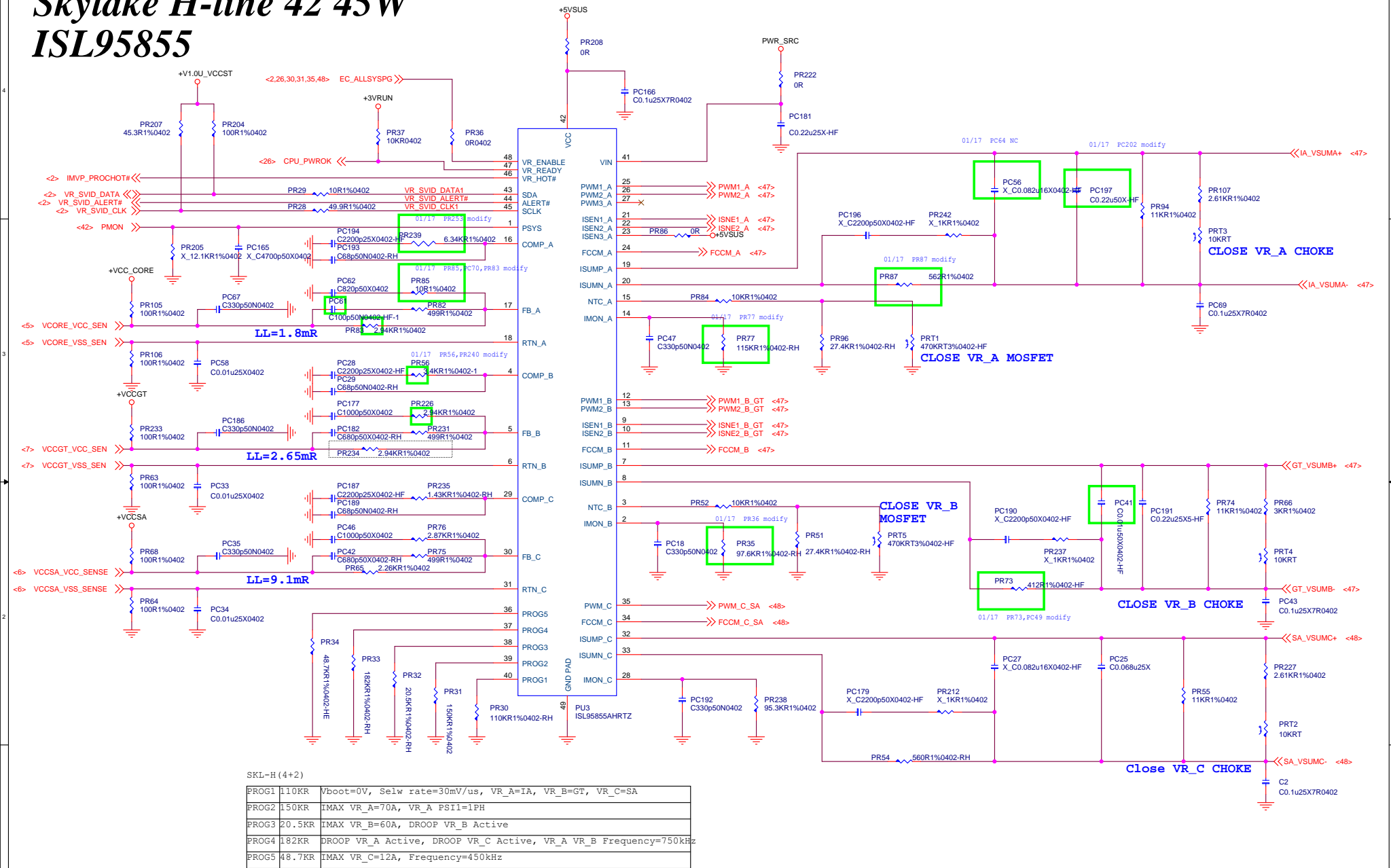
## +1V8\_SUS

Voltage = 1.8V  
Current = 1.6A  
OCP(Min) = 7A

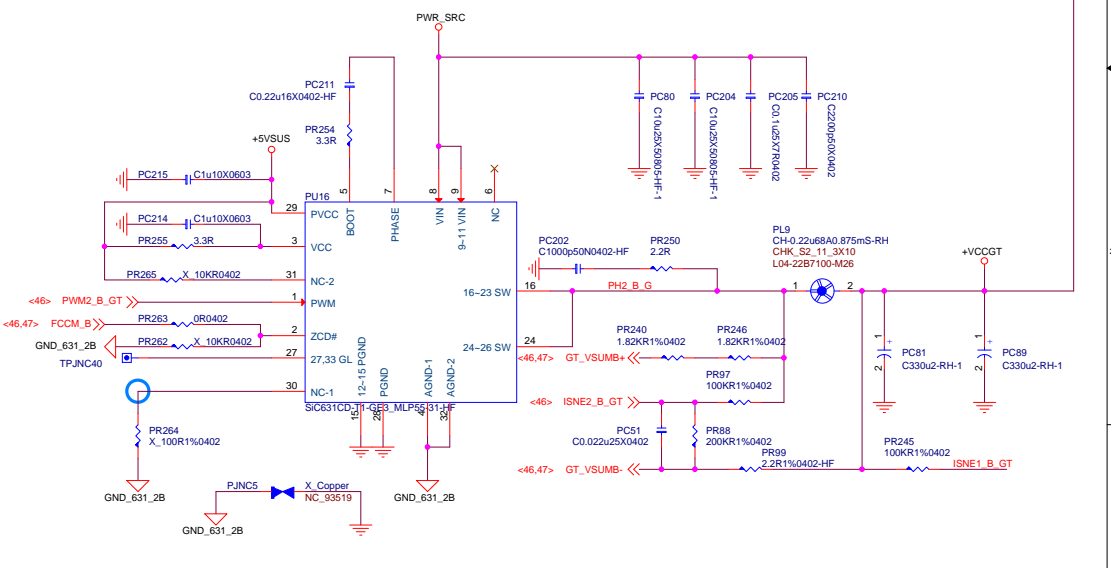
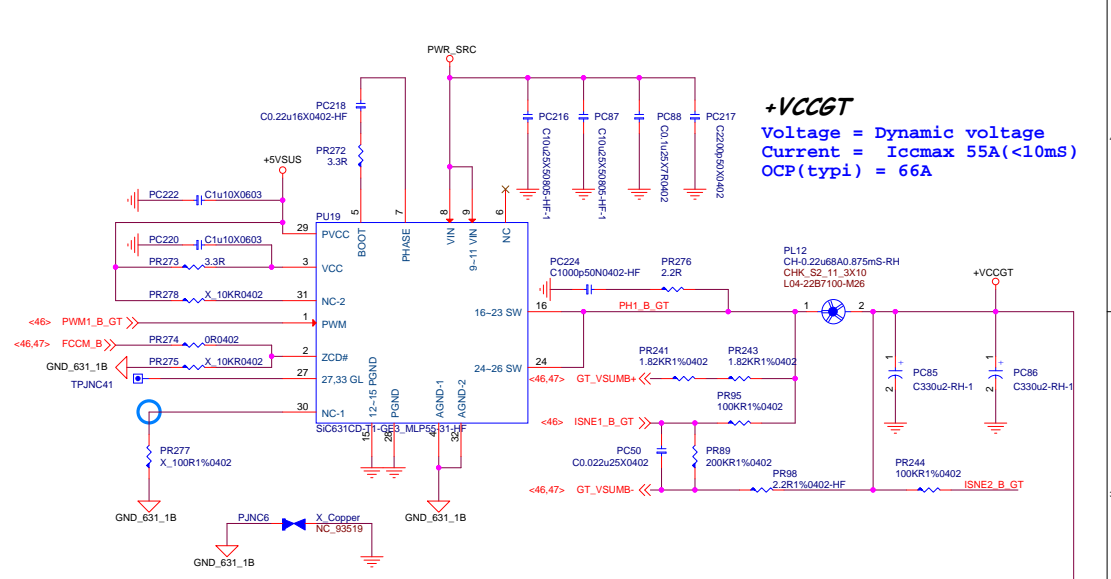


# Skylake H-line 42 45W

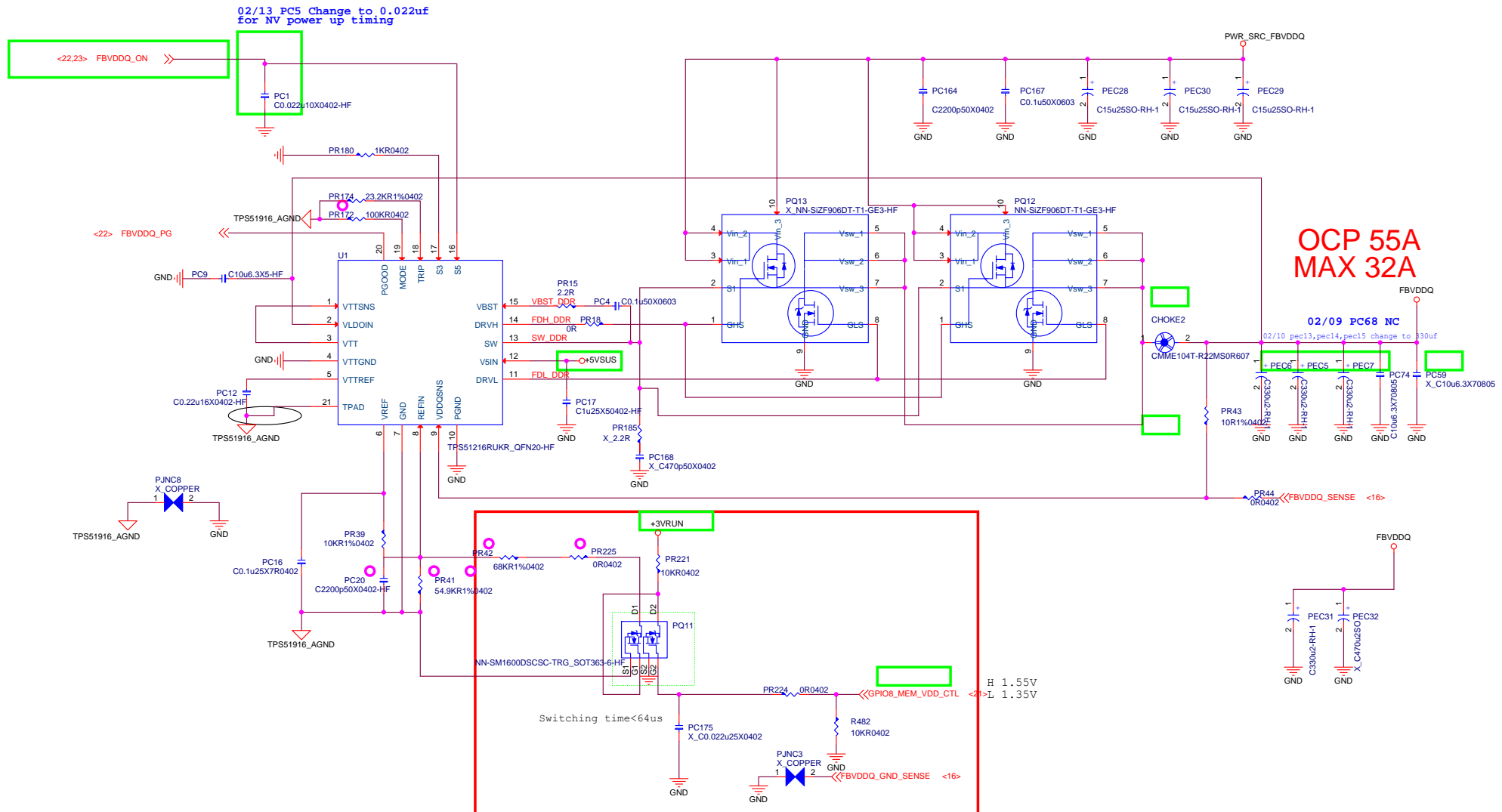
## ISL95855









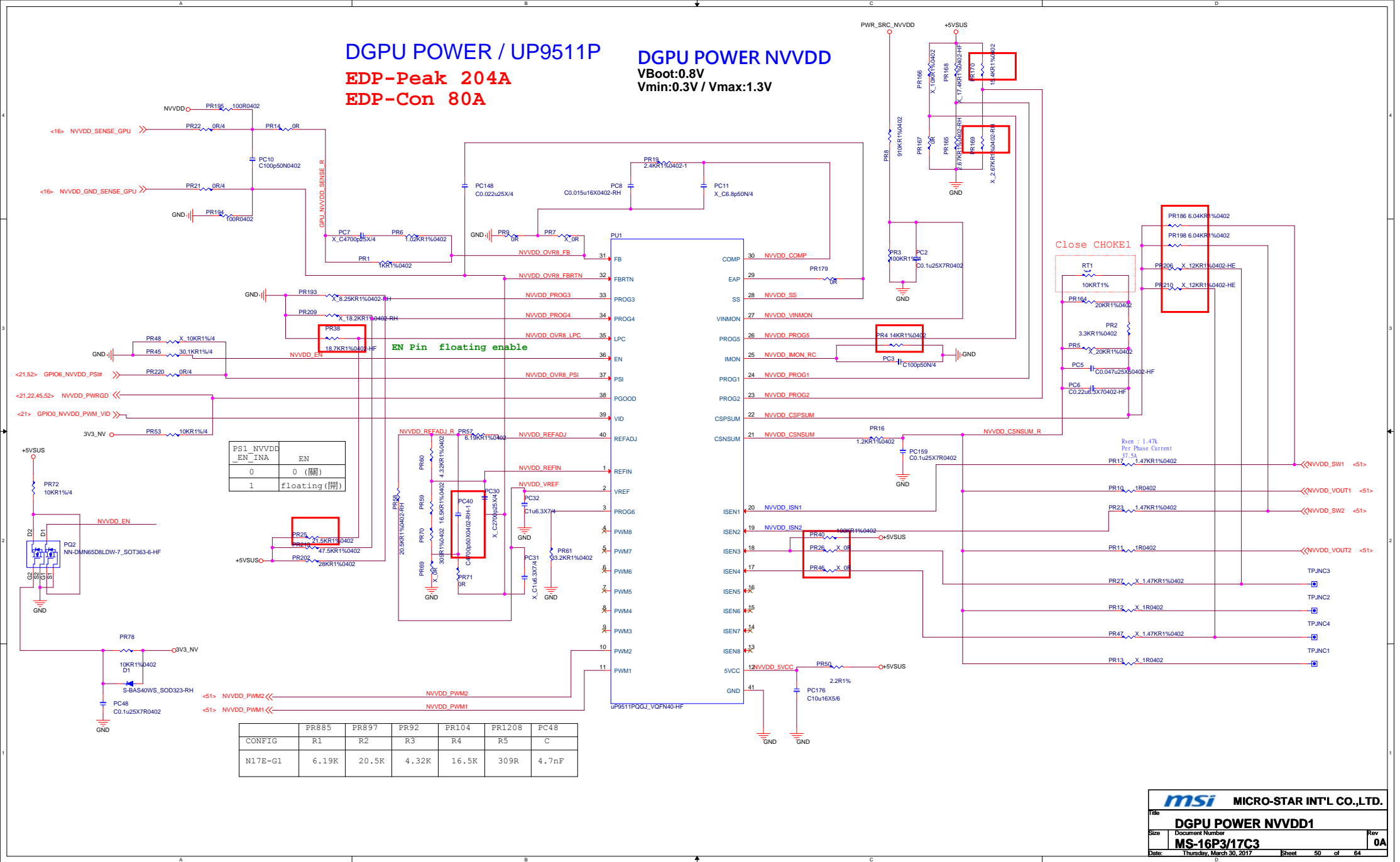


# DGPU POWER / UP9511P

EDP-Peak 204A  
EDP-Con 80A

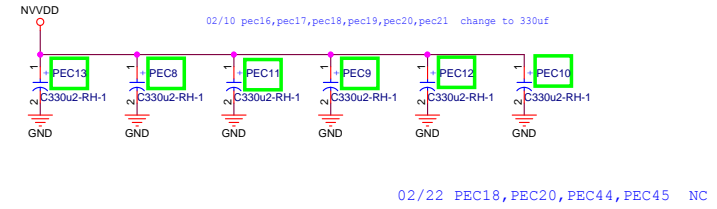
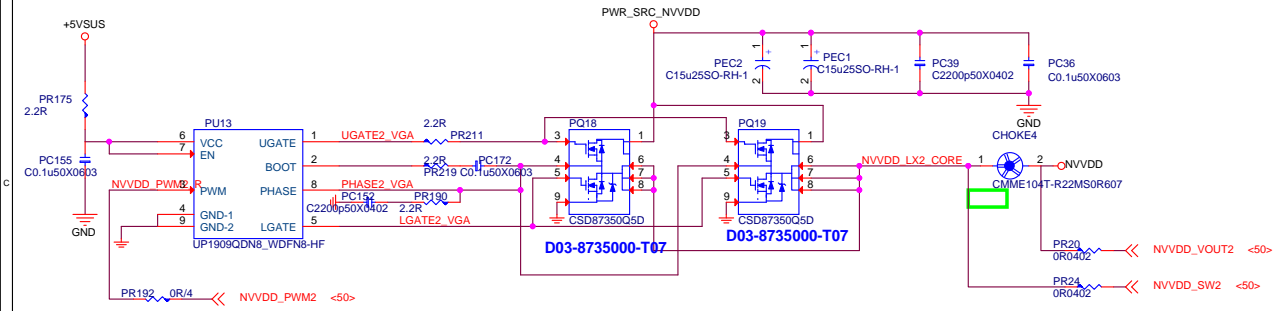
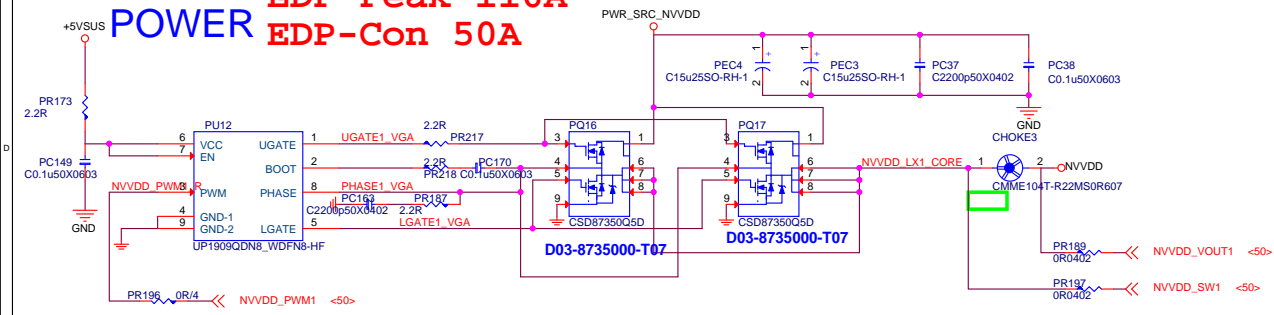
## DGPU POWER NVVDD

VBoot:0.8V  
Vmin:0.3V / Vmax:1.3V



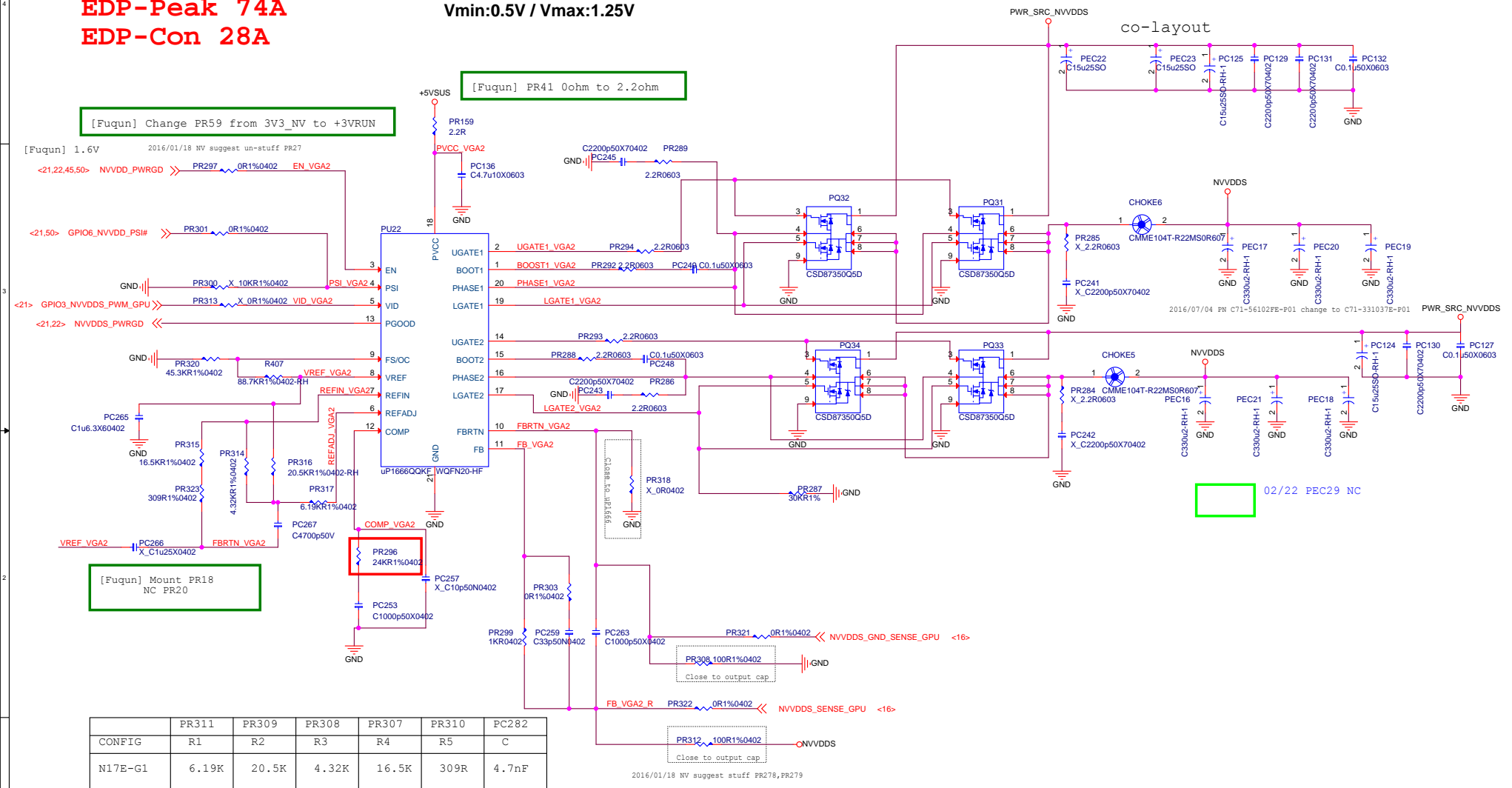
# DGPU POWER

EDP-Peak 116A  
EDP-Con 50A

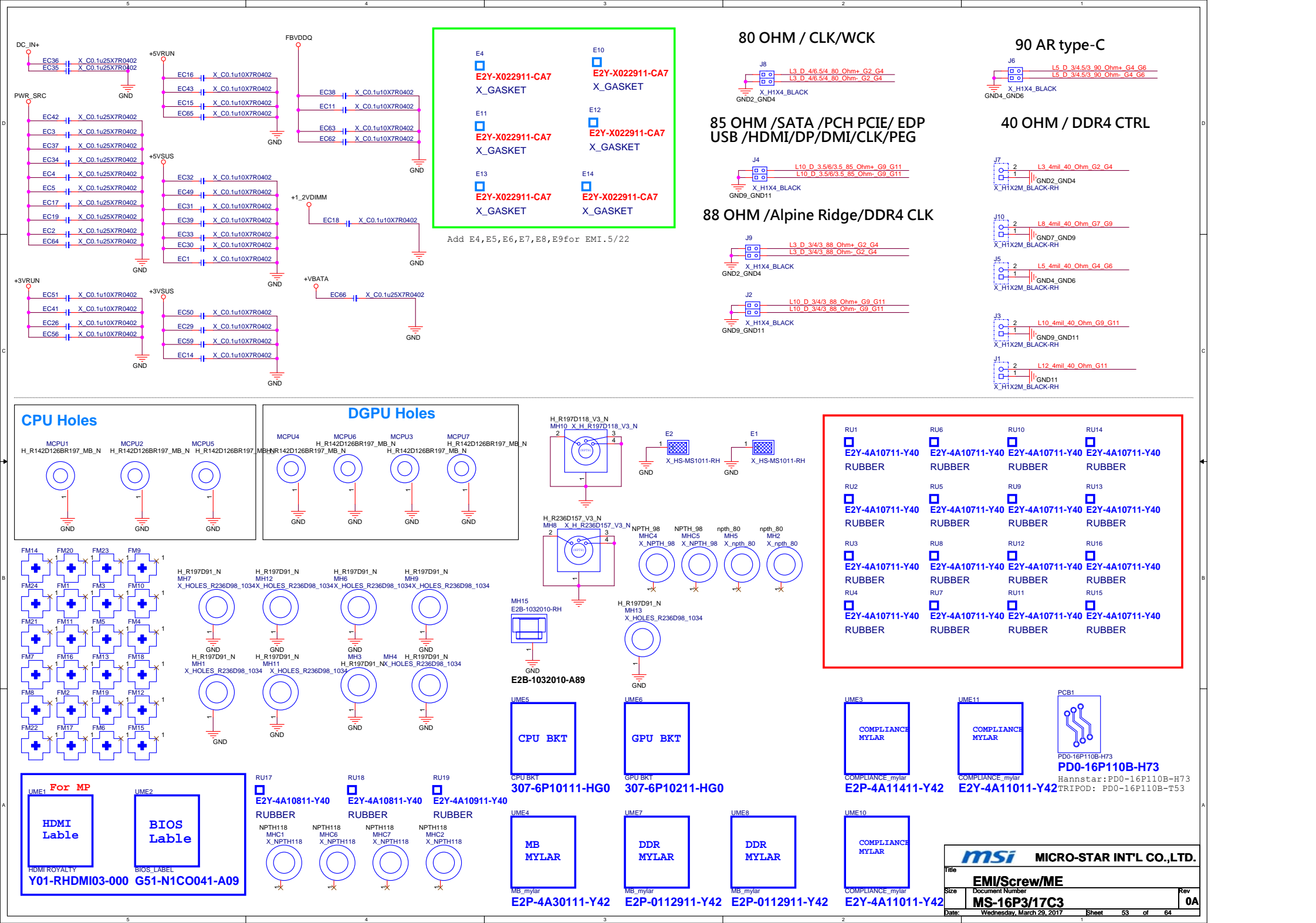


EDP-Peak 74A  
EDP-Con 28A

**VBoot:0.8V**  
**Vmin:0.5V / Vmax:1.25V**



	PR311	PR309	PR308	PR307	PR310	PC282
CONFIG	R1	R2	R3	R4	R5	C
N17E-G1	6.19K	20.5K	4.32K	16.5K	309R	4.7nF

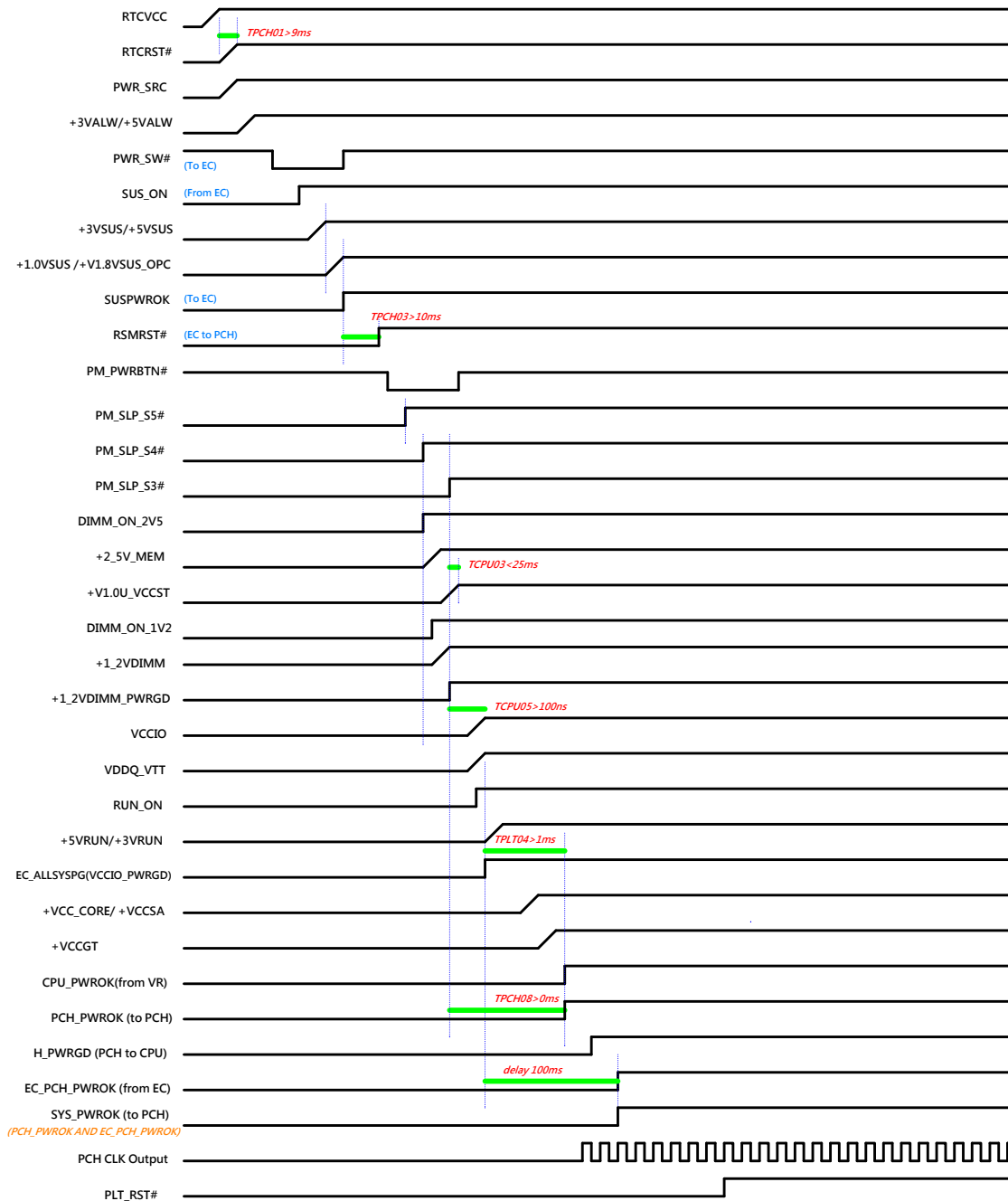




# MS-16P1 Power Delivery Chart

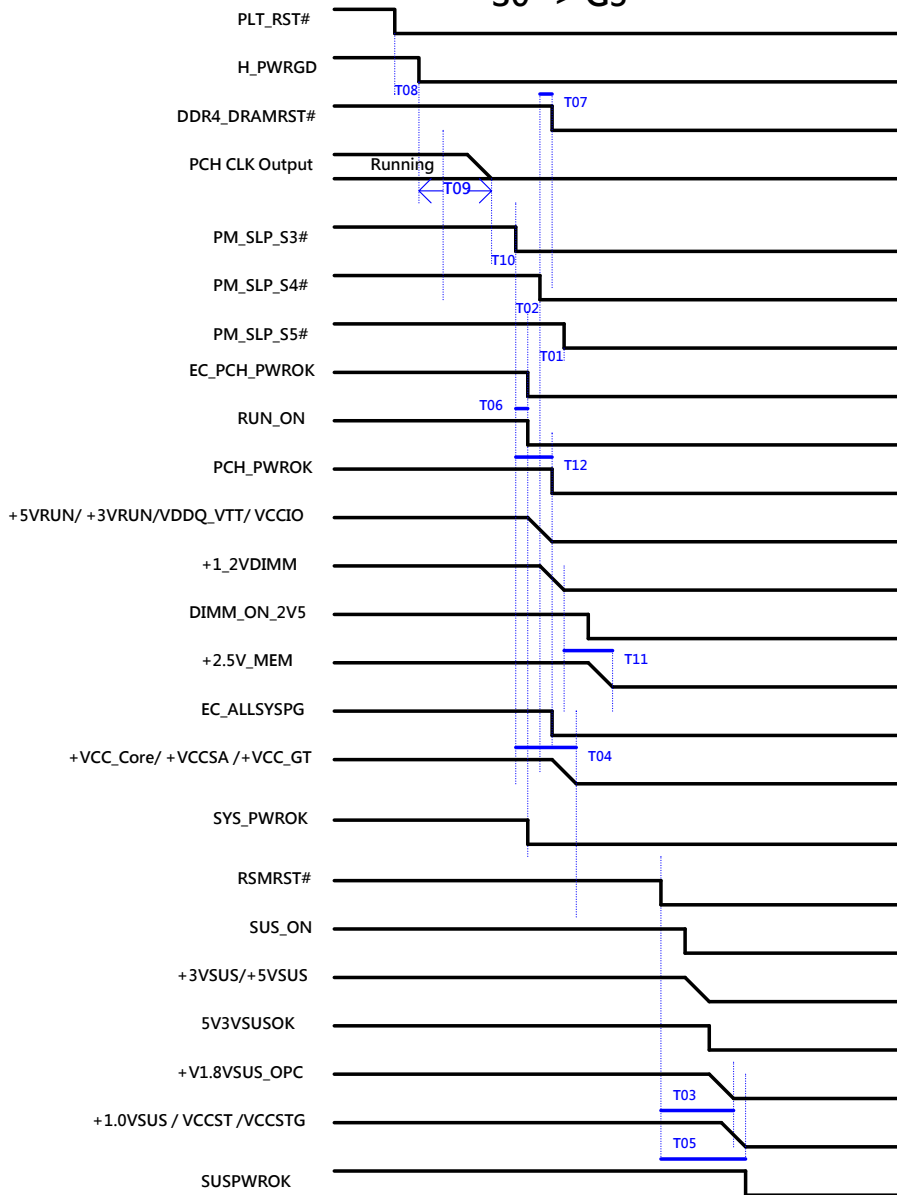
# Power on Sequence

G3 -> S0



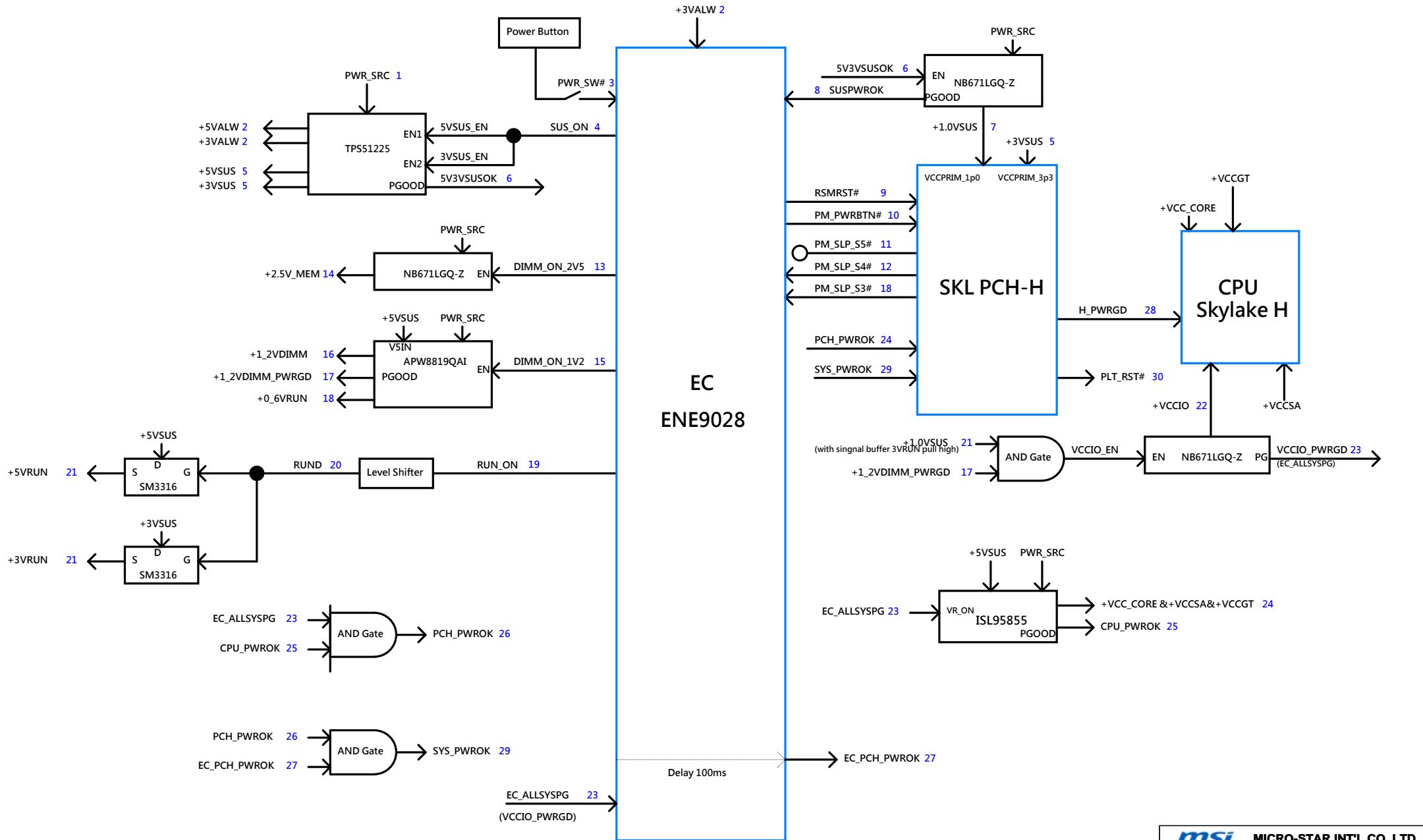
# Power down Sequence

S0 -> G3



	MIN	MAX	Units	Description
T01	30		us	SLP_S5# assertion to SLP_S4#
T02	30		us	SLP_S4# assertion to SLP_S3#
T03	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T04		500	ms	SLP_S3# assertion to VCC, VCCGT, VCCIO and VCCSA rails completely off.
T05	1		us	RSMRST# asserting to VccPRIM dropping 5% of nominal value
T06		1	us	SLP_S3# assertion to VCCIO VR disabled
T07	-100		ns	DDR_RESET# assertion to SLP_S4# assertion
T08	30		us	PLTRST# assertion to PROCPWRGD deassertion
T09	10		us	PROCPWRGD de-assertion to CLKOUT_BCLK turning OFF.
T10	1		us	CLKOUT_BCLK turning OFF to SLP_S3# assertion
T11	30		ms	VDDQ ramped down to VPP ramp down
T12	0		ms	SLP_S3# assertion to PCH_PWROK deassertion

# MS-16P1 Power on Block Diagram



OB:

2017/01/03

- 1. PCES P/N change to C71-33102AE-P01 on page59.
- 2. PQ47, PQ11, PQ9, PQ36, PQ10, PQ45 P/N change to D03-138DW19-D07 on page33, 52, 57..
- 3. R88, PR135, R64, PR140, R70, PR314, PR326 modify resistor value on page33, 57

2017/01/12

- 1. C175,C176,C177,C180,C181,C260,C285 P/N change to C11-4767314-M09 on page25.
- 2. Add PC275,PC276 on page 59
- 3. C370,C373 Change to 47uf/0805 on page10,27
- 4. Add +1.2VRUN page58
- 5. Add HDMI Retimer page46

2017/01/16

- 1. CN12 change to N53-09M0681-AF2

2017/01/17

- 1.PR150,PR148 改51.1K R11-5112T12-Y01
- 2.PR295 上件
- 3.PC237 改2.2nF C11-2222022-Y01
- 4.PR253 改3K R11-0302T12-Y01
- 5.PR85 改 10K R11-0100T12-Y01
- 6.PC70 改 100p C11-1011042-M09
- 7.PR83 改 2.94K R11-2941T12-Y01
- 8.PR66 改 3.48K R11-0342T12-Y01
- 9.PR240 改 2.94K R11-2941T12-Y01
- 10.PC66 改 NC不上件
- 11.PC202 改 0.22uF C11-2242813-Y01
- 12.PR87 改 562K R11-5620T12-Y01
- 13.PR77 改1.5K R11-1153T12-Y01
- 14.PR36 改 97.6K R11-9762T12-Y01
- 15.PR73 改412R R11-4120T12-Y01
- 16.PC49 改0.01uF C11-1032822-Y01

- 17.CN14,CN15 change to M15-0670320-CK3

2017/01/20

- 1. CN12 change to N53-13M0031-L06
- 2. Add Q40 for USB3.0LED

2017/01/23

- 1. PR108 change to 169K
- 2. Modify U64 pin17,18 Pin defin

2017/01/25

- 1. Modify CN12 pin define

2017/02/06

- 1. R481 NC,R483 上件
- 2. Add LED7 for17"

2017/02/08

- 1. R86,R93 change to 0603

2017/02/09

- 1. Add CN17,add A\_LED\_SCL,A\_LED\_SDA net
- 2. U28 modify HP\_SEL

2017/02/10

- 1. Add SW5,SW7 for 17"
- 2. Delete E7
- 3. C438,C840,C944,PEC13,PEC14,PEC15,PEC16,PEC17,PEC18,PEC19,PEC20,PEC21 change to 330uf
- 4. R895,C857 上件
- 5. R279,C834 modify for EMI
- 6. Add R614,R615

2017/02/13

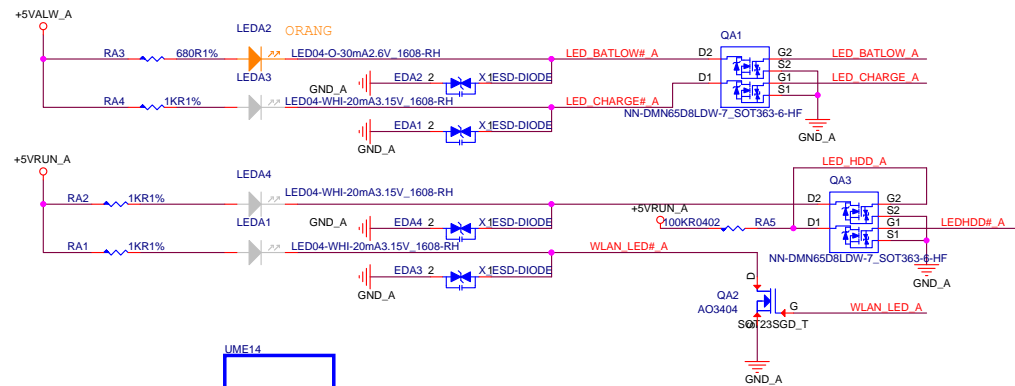
- 1. C856,C797,C777,C795 change to C11-1062617-S02
- 2. PC5 Change to 0.022uf

2017/02/14

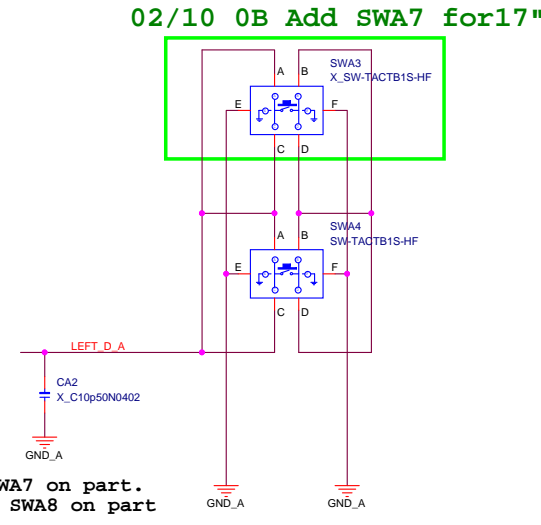
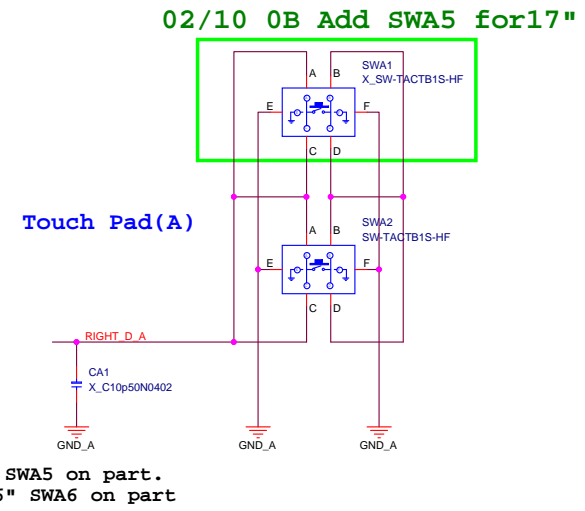
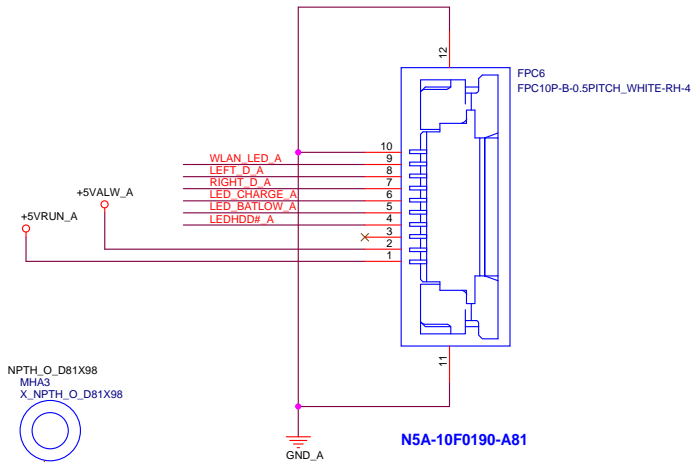
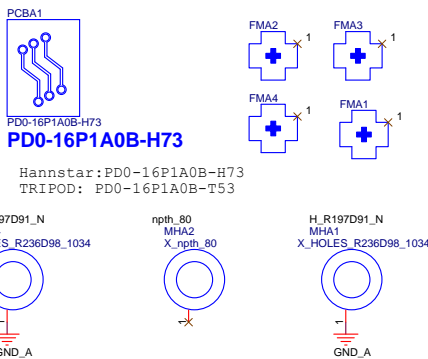
- 1. Add Q43,Q45,Q46 for audio impedance sense

2017/02/17

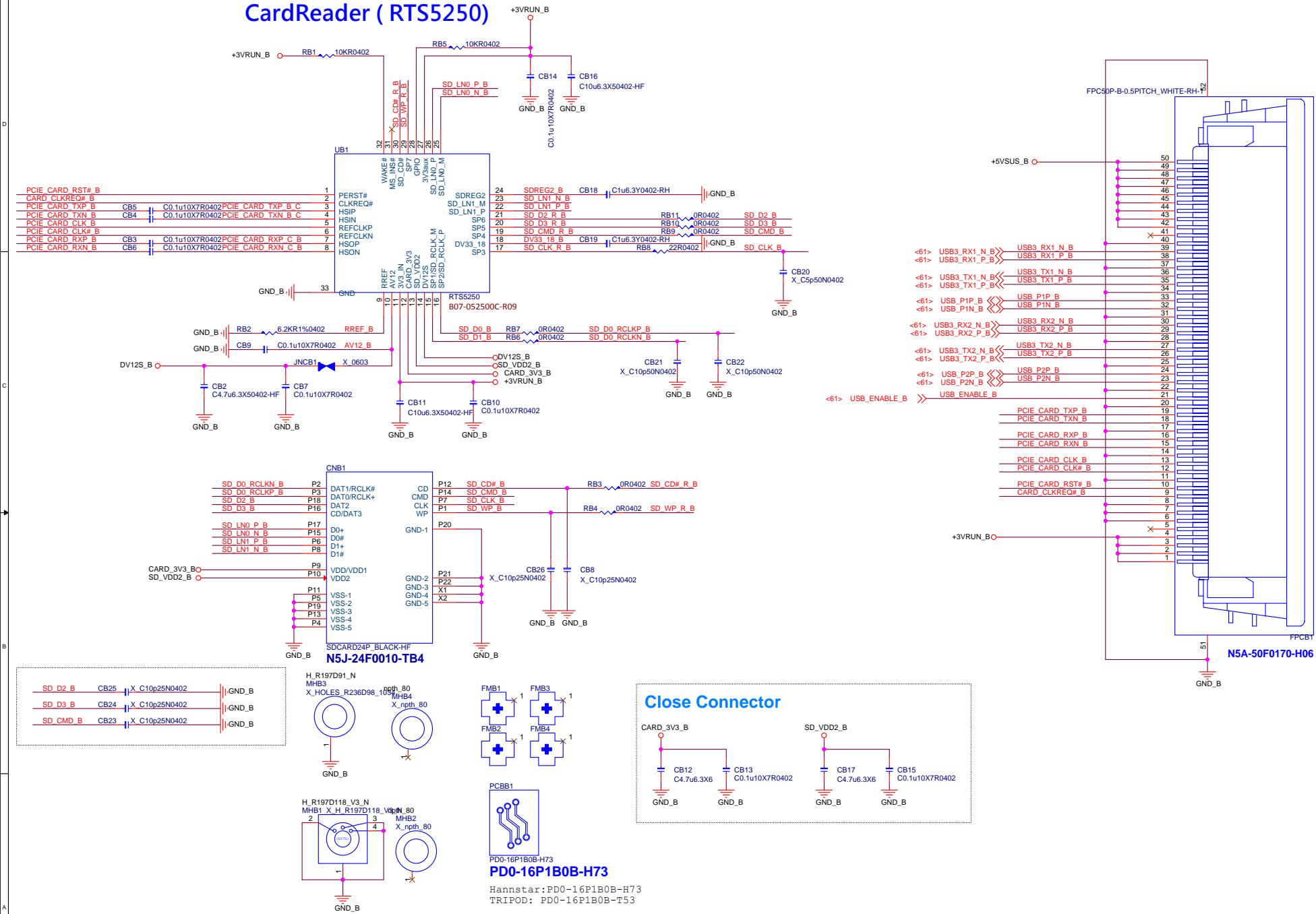
- 1. R242,R236,R235,R246,R234,R233 change to 0R
- 2. R165 NC,R170 上件



UME14  
**MB**  
**MYLAR**  
 POWER ADHESIVE  
**E2Y-6P11111-Y42**

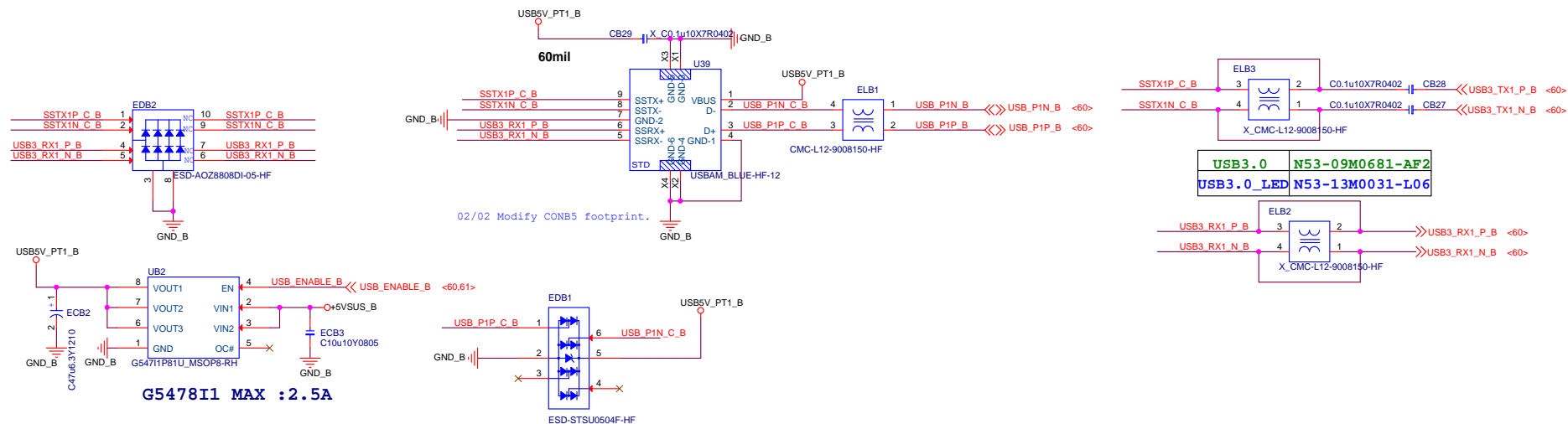


## CardReader ( RTS5250)

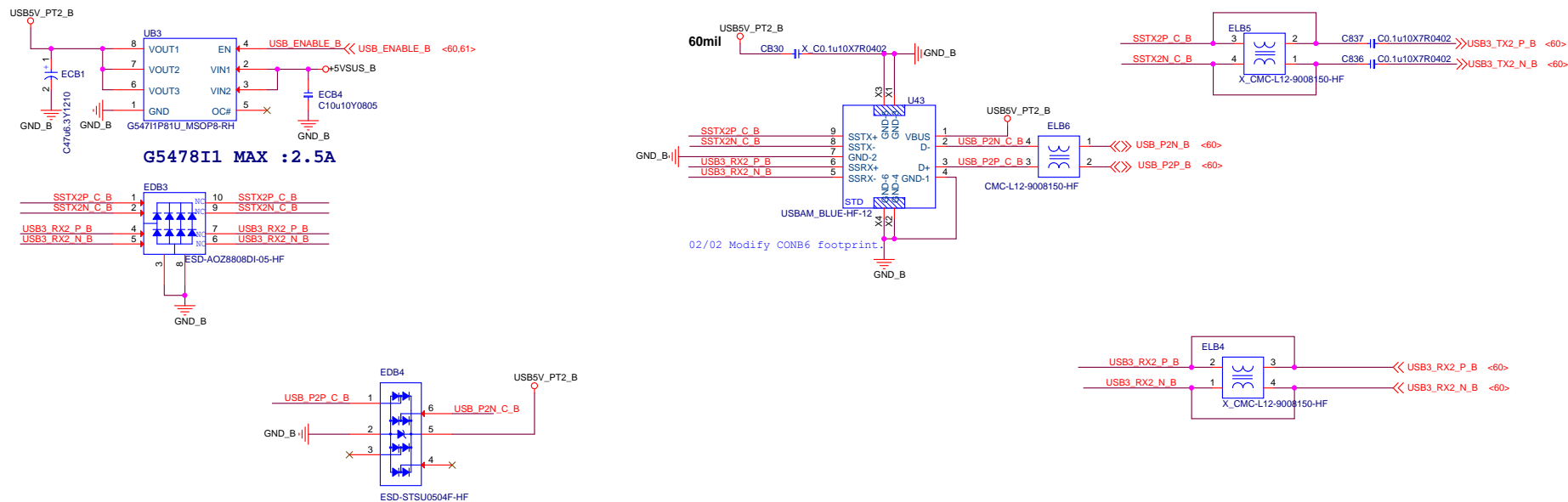




## USB2.0/USB 3.0

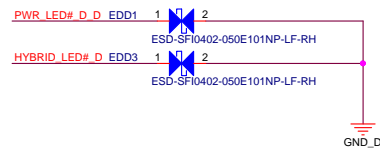
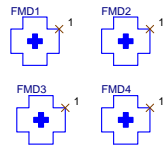
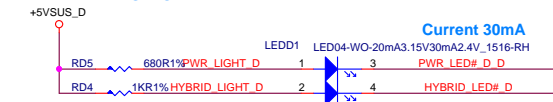


## USB 3.0 CNT 2



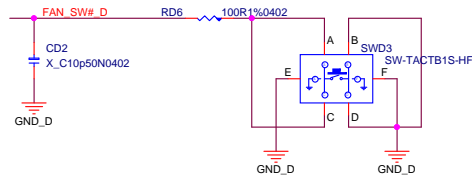
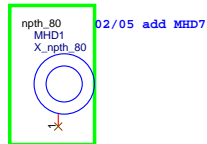
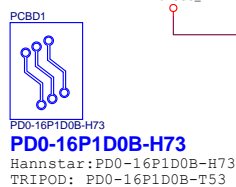
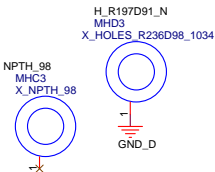
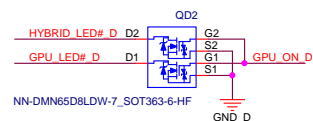
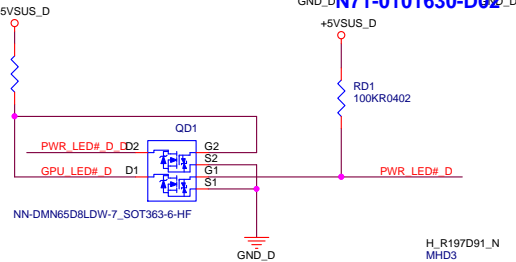
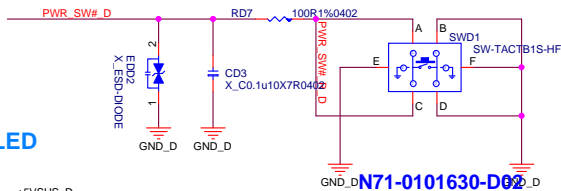
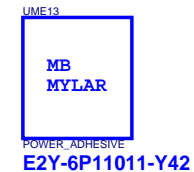
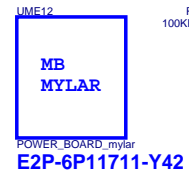
## Power LED

Current 30mA

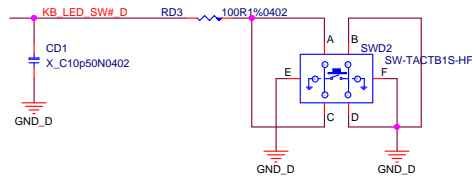


## Power Switch

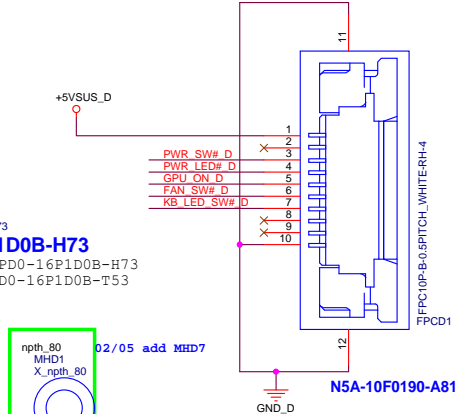
## Control PWR LED



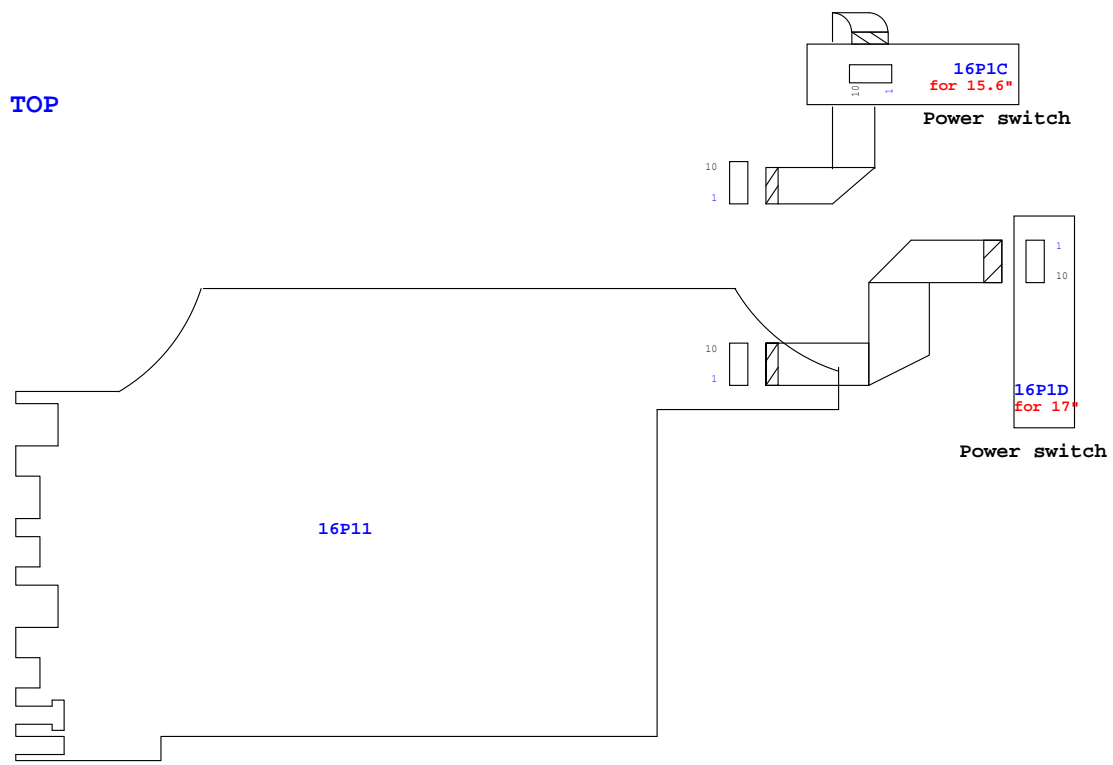
N71-0101630-D02



N71-0101630-D02



TOP



Bottom VIEW

